6.780
Semiconductor Manufacturing
Spring 2003

Problem Set #6

Issued: Wednesday, April 2, 2003
Due: Monday, April 7, 2003

Problem 1

Do problem 1 in May & Spanos, Chapter 5, as repeated below.

Assuming a Poisson model, calculate the maximum defect density allowable on 100,000 NMOS transistors in order to achieve a functional yield of 95%. Assume the gate of each device is 10 μm wide and 1 μm long.

Problem 2

Do problem 5 in May & Spanos, Chapter 5, as restated below (wording change in italics).

10,000 units of a product with area 0.5 cm^2 and 200 chips per wafer are to be produced in three manufacturing areas *(each wafer passes through all three of these manufacturing areas in turn)*, with a D_0 of 0.9, 1.1, and 1.3 cm^{-2}, respectively. How many wafers need to be ordered? Assume a negative binomial model with $\alpha = 2$ and a combined fabrication, assembly, and test yield of 95%.

Problem 3

Do problem 4 in May & Spanos, Chapter 5, as repeated below *with modifications*. This problem is based on the figure and discussion in the paper by Stapper and Rosner, which may help to refer to. Note that the bounds on the first equation have been modified from that in May & Spanos to match Fig. 5 in Stapper.

Consider the effect of defects on IC interconnect. Figure P5-4 below illustrates the impact of defect size on critical area for circular defects of diameter *x*.

The area in which the center of such defects must fall to cause a failure increases linearly as a function of defect size. It can be expressed as

$$A_c(x) = L(x + W - 2R)$$

$$W - R \le x \le \infty$$

where *L* is the interconnect length and *R* is the *minimum remaining width* in the interconnect line. Suppose that the normalized probability density function of defect sizes is given by

$$g(x) = \frac{X_U^2 \cdot X_L^2}{x^3 (X_U^2 - X_L^2)}$$

where X_L^2 and X_U^2 are the lower and upper limits of the range of defect sizes, respectively.

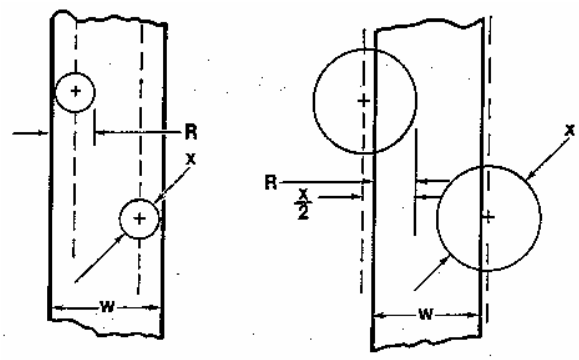

Figure P5-4

(a) Find an expression for the average critical area (A_{AV}) by evaluating the integral

$$A_{AV} = \int_{X_L}^{X_U} A_c(x)g(x)dx$$

(b) *Find an expression containing only L, W, R, and X_L for the average critical area, in the limit* as the upper limit on defect size approaches infinity. *As the minimum wire remaining value (R) goes to zero, does your expression behave as you might expect?*

$$A_{AV} = \frac{L \cdot X_L^2 \cdot W}{R^2}$$

Problem 4

Do problem 10 in May & Spanos, Chapter 5, as repeated below.

Suppose that you use 200 mm wafers, and also assume that you can only get functional dice only within the inner 190 mm diameter (outer 5 mm margin is full of defects). On the one product that you have run so far, a chip 5 mm x 5 mm, the yield is 80%.

(a) Using the simple Poisson model, find the defect density (in the good area of the wafer) and plot the yield as a function of *S*, where *S* is the square root of the area of the die in production. Plot the total and the good die per wafer as a function of *S* on the same graph.

(b) Repeat the calculations and plots in (a) using the negative binomial model (α = 1.5).

(c) Suppose that an alternative explanation for the data were that some fraction, *f*, of the wafer was perfect and the rest was totally dead. This is the “black-white” model that assumes a perfect deterministic

clustering of defects. What is *f*? Plot the Good Die per wafer for this model on the same graph as in (a)-(b).

(d) What defect density reduction would you have to achieve to yield 50% of the available die at S = 15 mm according to models (a), (b) and (c)?

Problem 5

Prior characterization of a fab has been performed for two critical process layers. The metal3 layer has been found to have a random defect density of 1 cm^{-2}. The via3 process has a random failure rate of 10^{-7}.

A new product with a chip size of 2 mm x 4 mm is proposed to run on this fab line. A functioning chip will sell for $10. The product has both memory and logic blocks. The memory block has a critical area to metal1 failures of 3 mm^2, and has 2 x 10^6 vias. The logic, on the other hand, has a critical area to metal1 failures of 5 mm^2, but only 10^5 vias.

(a) Complete the following yield impact matrix (as in Ciplikas) for this product. As a reminder, the interior cells give the limited yield for that block and process step; the bottom columns give the aggregate yield for the process, the rightmost rows give the aggregate yield for the block, and the corner entry gives to aggregate chip yield.

	metal3	via3	
Memory Block			
Logic Block			

(b) You are the memory module integration engineer, and you are considering layout changes to the metal3/via3 design to improve the memory block yield. Experimentation in the fab has shown that for each 0.1 μm of border added around all vias in the design, the via3 failure rate decreases by a factor of 10. However, the extra borders cause the metal1 critical area to increase: specifically, each 0.1 μm of border added increases the critical area by 10%. How much, if any, border area should be added to the memory block vias, to optimize the memory block yield? Note that the vias borders can be selected in 10 nm (0.01 μm) increments.

(c) The fab manager is responsible for total income for the product through this 200 mm wafer fab. Given that any borders also increases the total die size by the same amount (i.e. each 0.1 μm added border adds 10% to the total die size), evaluate the reaction to your proposed product design modification in part b. If implemented (and assuming 100% yield in all other process steps), how much revenue per wafer would be gained our lost by your proposal?