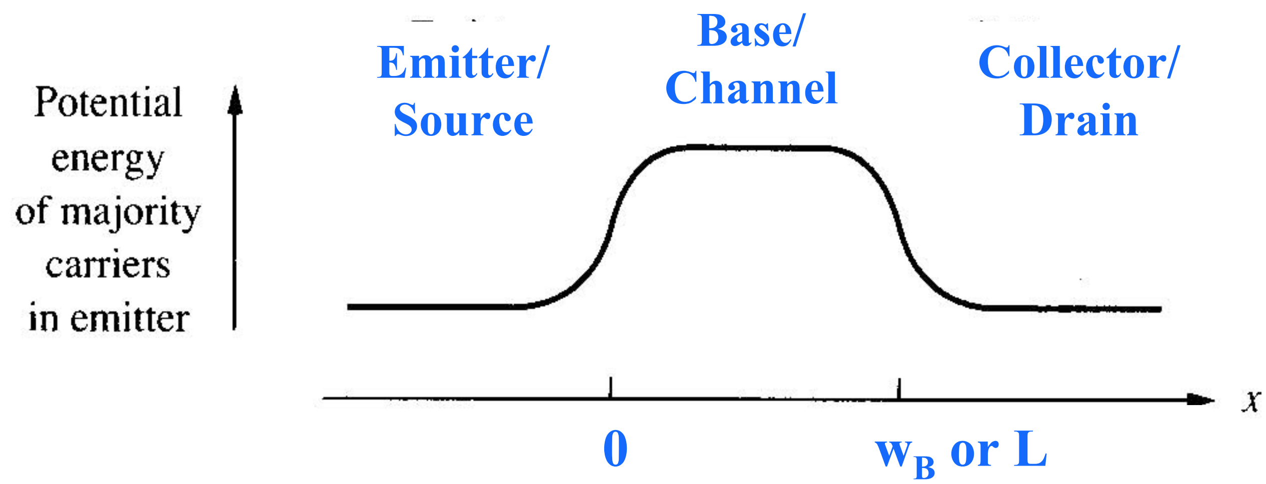
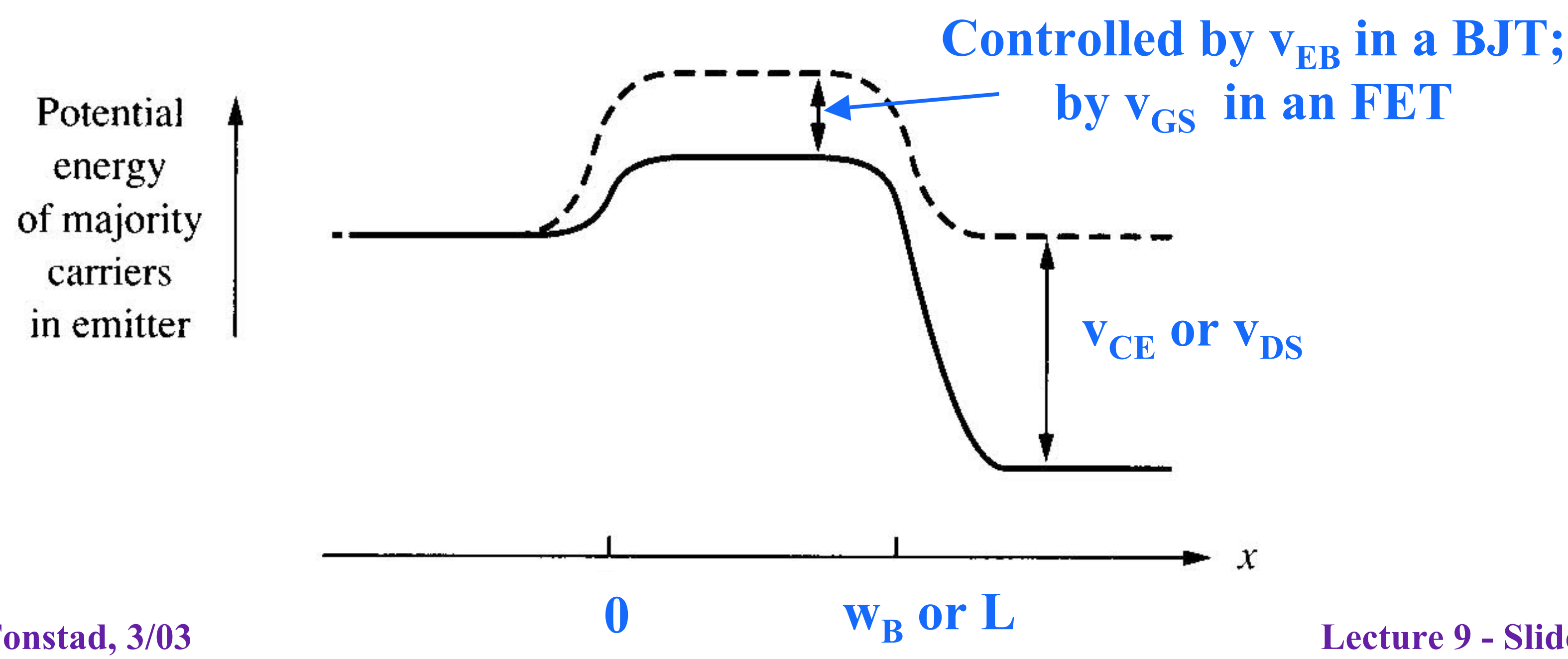
Lecture 9 - Metal-Semiconductor FETs - Outline

- **Device structure and operation**
  - Concept and structure:
    - General structure
    - Basis of operation; device types
  - Terminal characteristics
    - Gradual channel approximation w. o. velocity saturation
    - Velocity saturation issues
    - Characteristics with velocity saturation
    - Small signal equivalent circuits
  - High frequency performance
- **Fabrication technology**
  - Process challenges: (areas where heterostructures can make life easier and better)
    - 1. Semi-insulating substrate; 2. M-S barrier gate; 3. Threshold control; 4. Gate resistance; 5. Source and drain resistances
  - Representative sequences:
    - 1. Mesa-on-Epi; 2. Proton isolation; 3. n+/n epi w. recess; 4. Direct implant into SI-GaAs

BJT/FET Comparison - cont.





BJT/FET Comparison - cont.

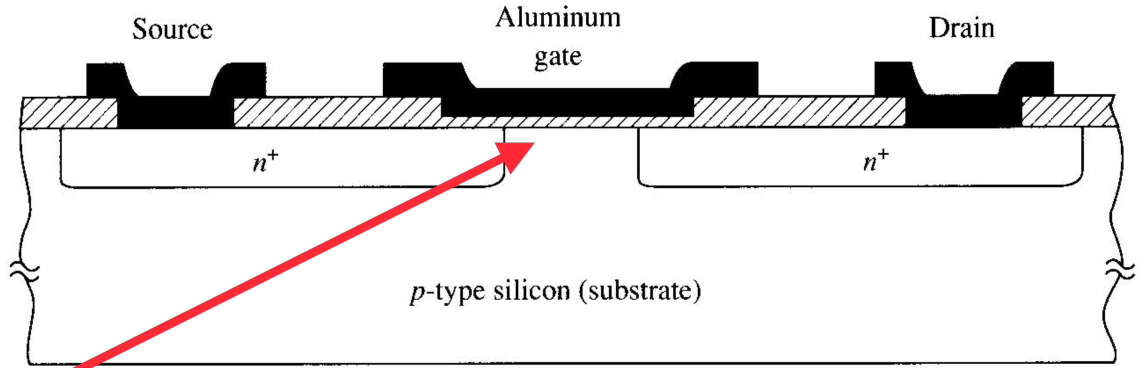
OK, that's nice, but there is more to the difference than how the barrier is controlled

	BJT	FET
Charge carriers	minority in base	majority in channel
Flow mechanism	diffusion in base	drift in channel
Barrier control	direct contact made to base	change induced by gate electrode

The nature of the current flow, minority diffusion vs majority drift, is perhaps the most important difference.

FET Mechanisms - MOSFET and JFET/MESFET

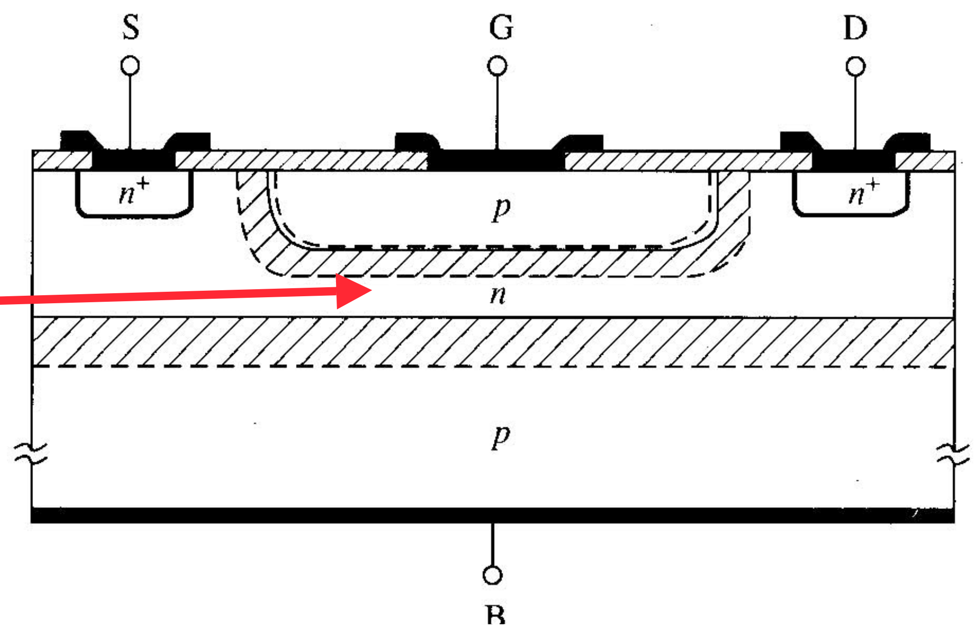
MOSFET



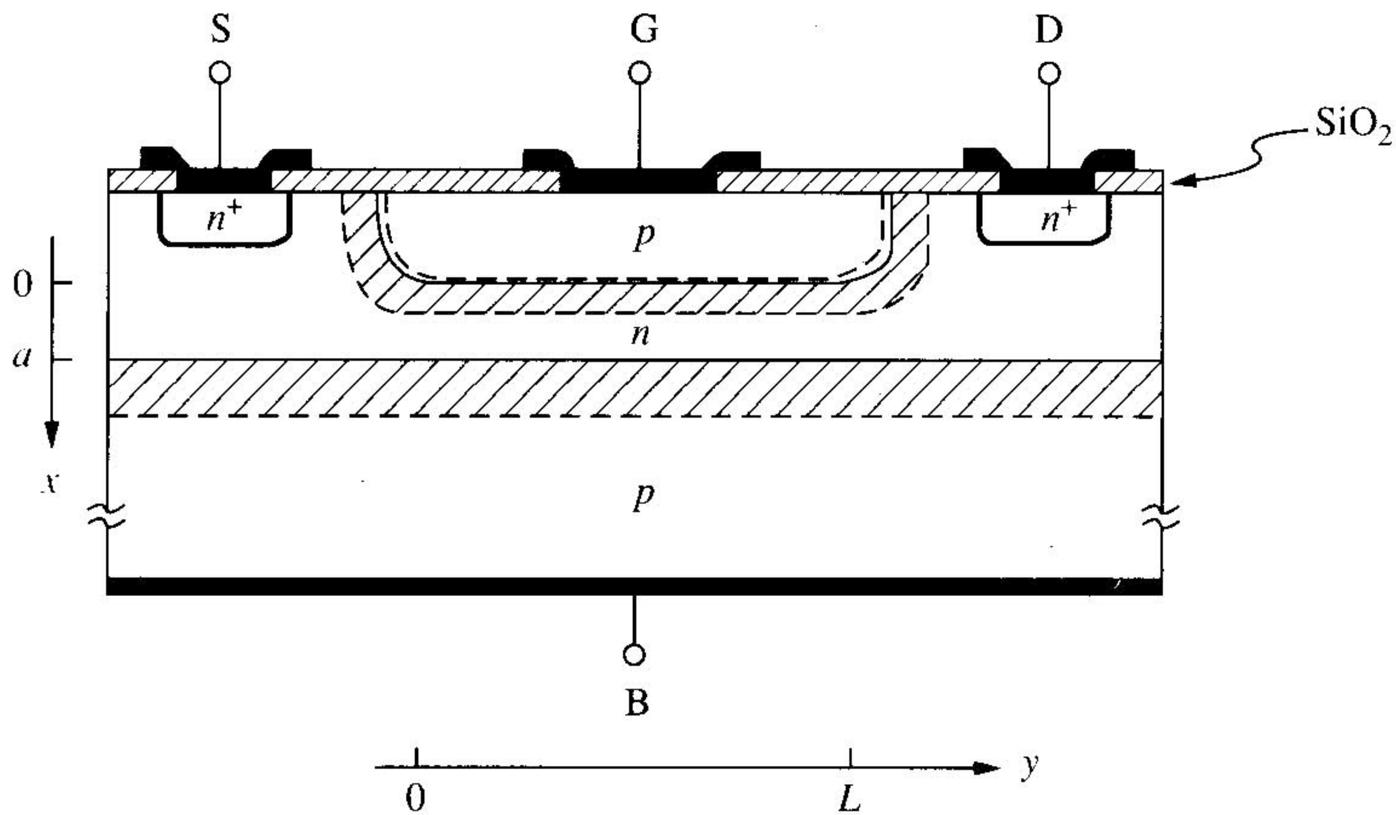
Induced n-type channel

JFET

Doped n-type channel



Junction Field Effect Transistor (JFET)



Reverse biasing the gate-source junction increases depletion width under gate and constricts the n-type conduction path between the source and drain.

JFET, cont.

Operating regions:

(a) linear (or triode) well below pinch-off

$V_p < v_{GS} < 0$, v_{DS} small

(b) linear nearing pinch-off

$V_p < v_{GS} < 0$, v

nearing (v_{GS} - $_p$)

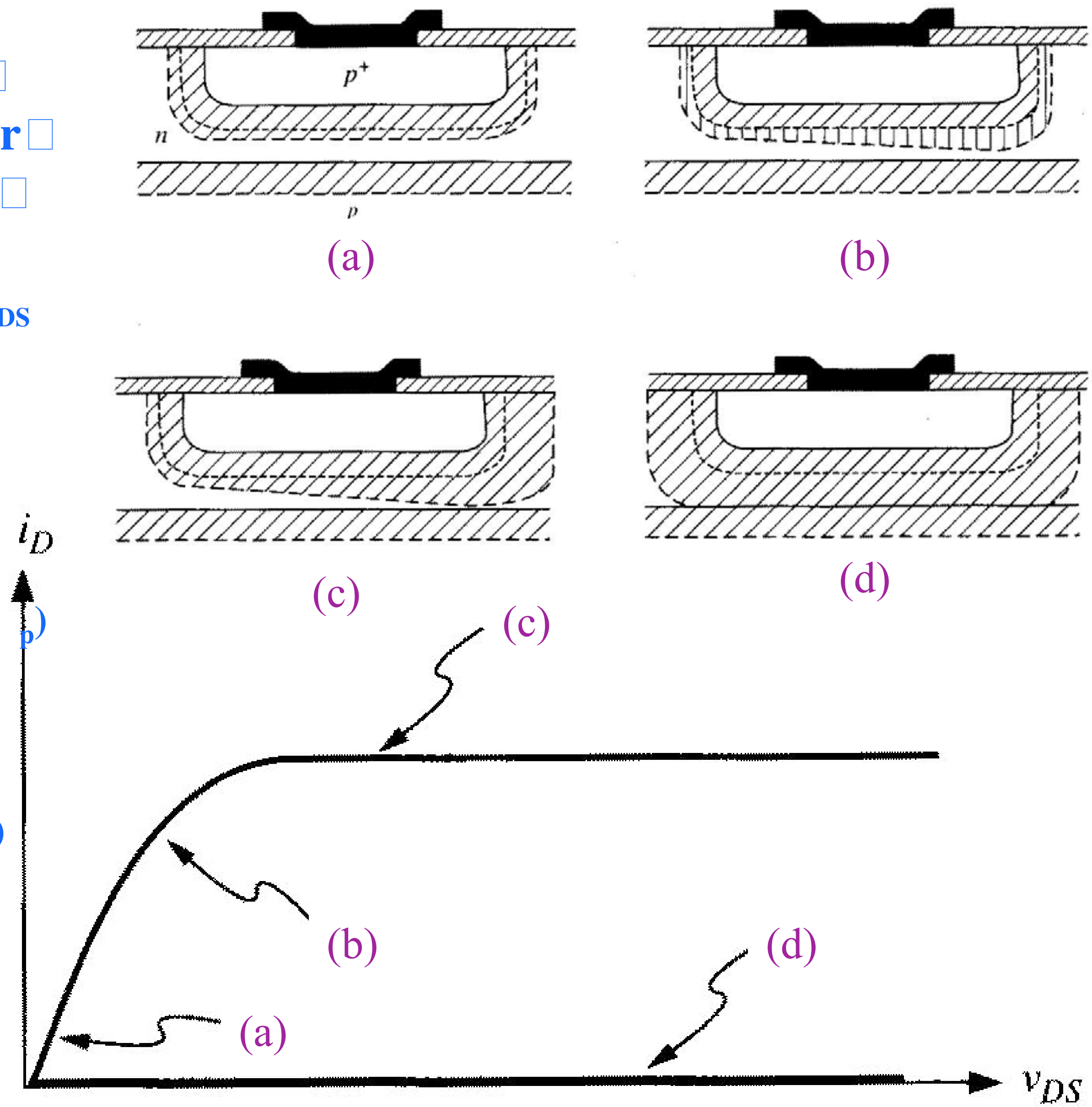
(c) pinch-o

$V_p < v_{GS} < 0$,

$v_{DS} > (v_{GS} - V_p)$

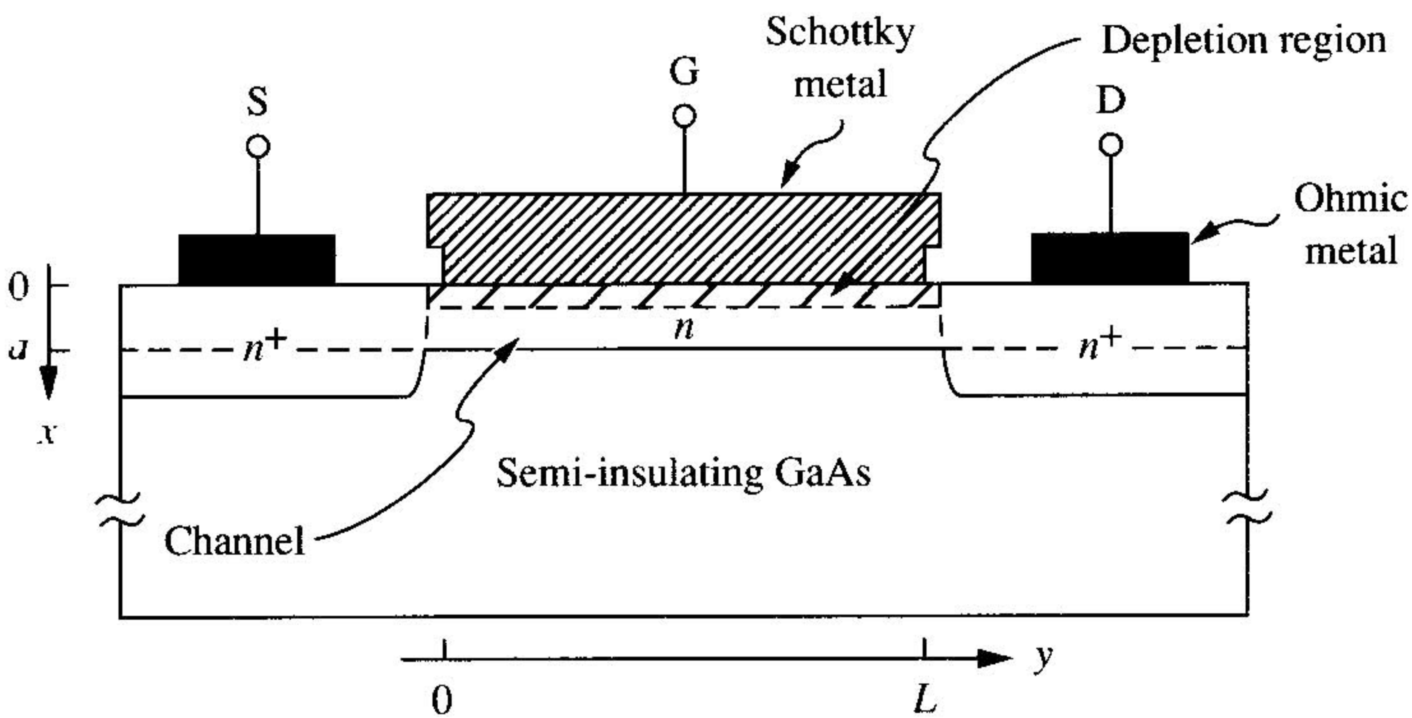
(d) cut-off

$v_{GS} < V_p < 0$



Ref: Fonstad, Chap. 10

MEtal Semiconductor FET - MESFET



The operation is very similar to that of a JFET. The p-n junction gate is replaced by a Schottky barrier, and the lower contact and p-n junction are eliminated because the lightly doped p-type substrate is replaced by a semi-insulating substrate.

MESFET current-voltage (i-v) characteristic

We have two currents, i_G and i_D, that we want to determine as functions of the two voltages, v_{GS} and v_{DS}:

$$i_g(v_{gs}, v_{ds}) \quad and \quad i_d(v_{gs}, v_{ds})$$

If we restrict our model to drain-to-source voltages greater than zero, and gate-to-source voltages less than the turn-on voltage of the gate Schottky diode, then, say that the gate current is negligible and $i_G \approx 0$:

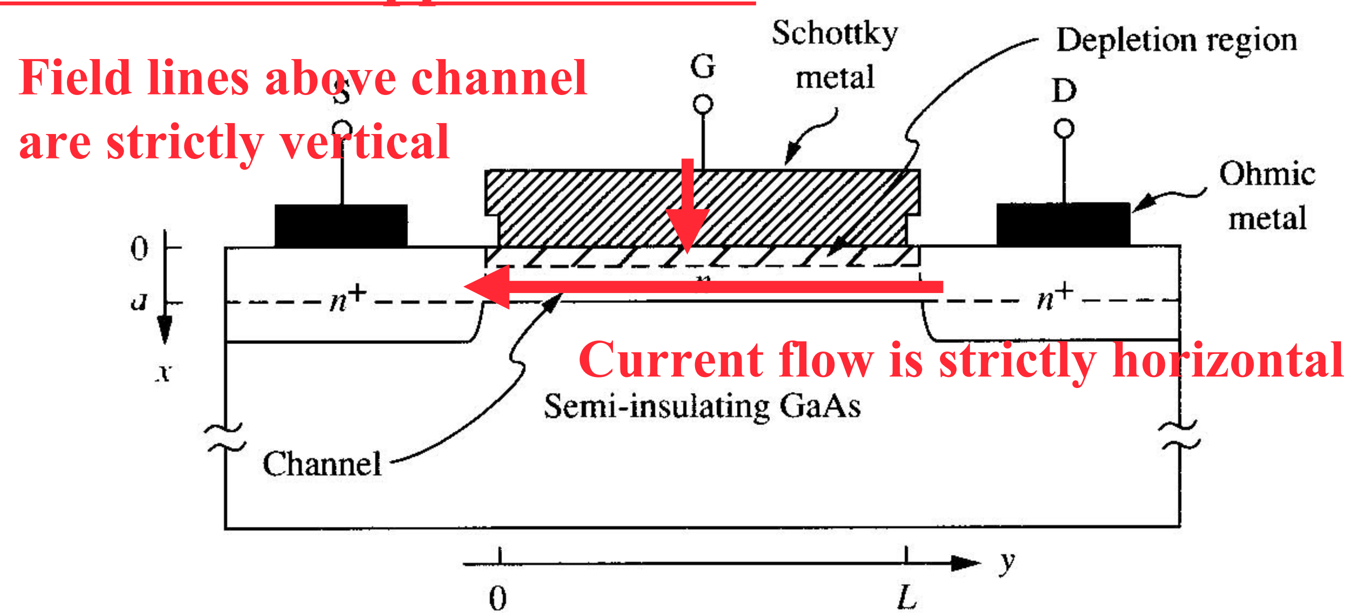
$$i_g(v_{gs}, v_{ds}) \approx 0 \quad if \quad v_{gs} \leq V_{on}, \; and \; v_{ds} \geq 0.$$

Our real problem then is to find an expression for the drain current, i_D. The path for the drain current is through the channel to the source, and we model it using the gradual channel approximation (next slide).

MESFET current-voltage (i-v) characteristic

The model used to describe the drain current-voltage expression for an FET is the Gradual Channel Approximation. In this model we assume the current flow in the channel is entirely in the y-direction, and that the field lines terminating on the gate are entirely vertical.

Gradual Channel Approximation

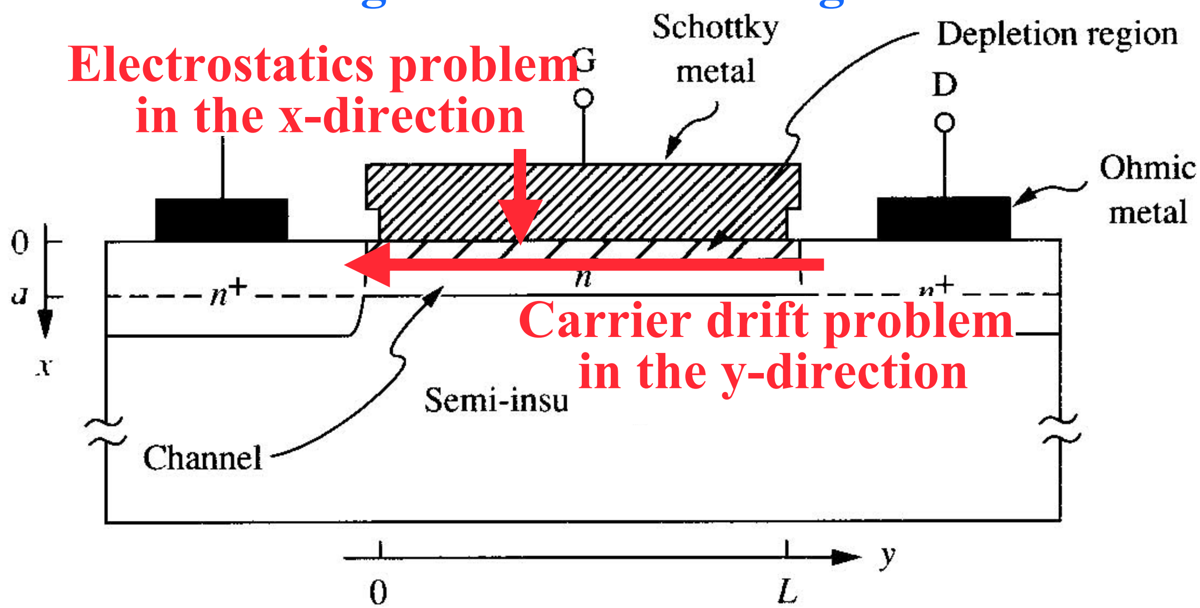


MESFET i-v: gradual channel approximation

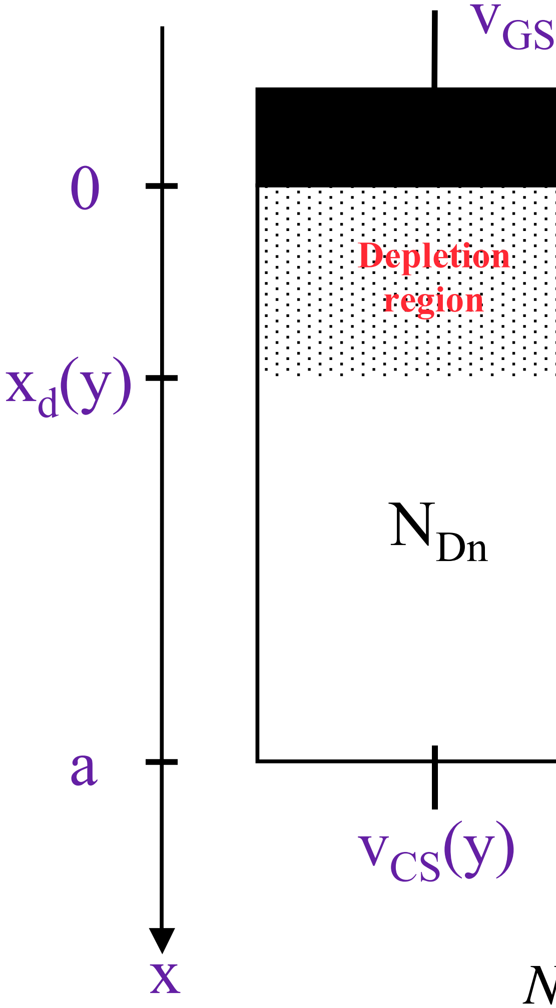
If the Gradual Channel Approximation is valid we can solve two independent 1-d problems in sequence:

(1) an electrostatics problem in the vertical (x-) direction to find the mobile charge sheet density at any point, y, in the channel;

(2) a drift problem in the horizontal (y-) direction to relate the voltage drop along the channel to the current. We integrate this relation from y = 0 to y = L to get the final expression relating the drain current to the gate and drain voltage.



MESFET i-v: vertical electrostatics problem



The sheet carrier density at the position y along the channel is:

$$N_{ch}(y) = N_{Dn}\left[a - x_d(y)\right]$$

And the depletion width there is:

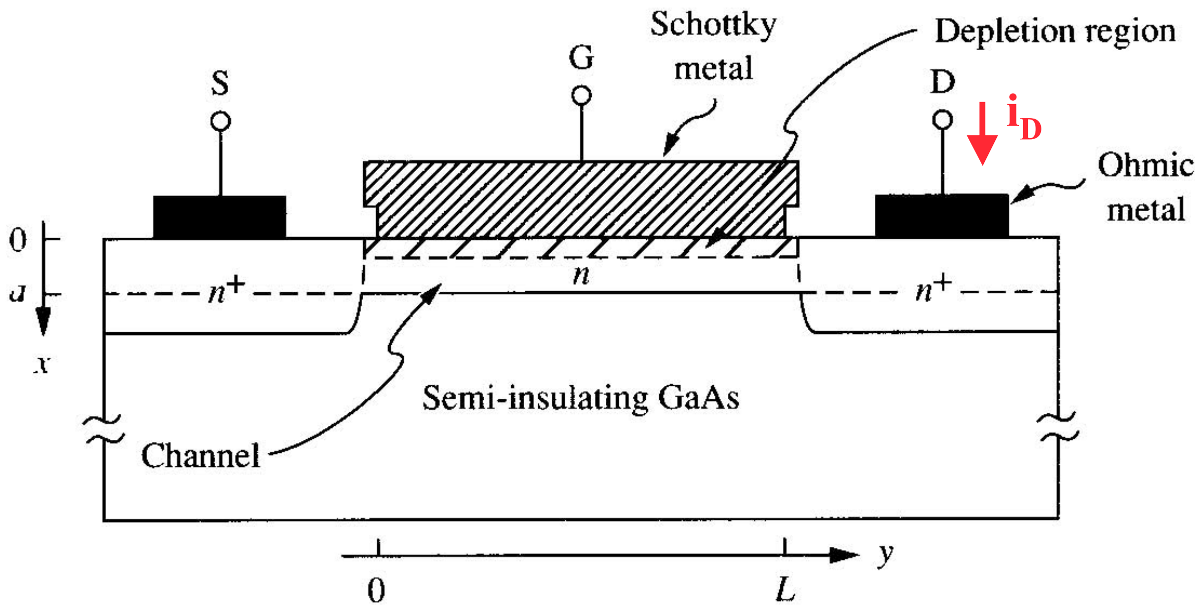
$$x_d(y) = \sqrt{2\varepsilon_S\left\{\phi_b - \left[v_{GS} - v_{CS}(y)\right]\right\}/qN_{Dn}}$$

Combining these yields:

$$N_{ch}(y) = N_{Dn}\left[a - \sqrt{2\varepsilon_S\left\{\phi_b - \left[v_{GS} - v_{CS}(y)\right]\right\}/qN_{Dn}}\right]$$

This is the information we wanted to get from the vertical problem.

MESFET i-v: horizontal drift current problem



- Define $v_{CS}(y)$ as the voltage in the channel relative to the source at y.
  $v_{CS}(y)$ varies from v_{DS} at y = L to 0 at y = 0
  the horizontal E-field in the channel, E_y, is $- dv_{CS}(y)/dy$

- The drain current, i_D, flows right to left in the channel:
  - i_D is a constant and is not a function of y
  - at any y, i_D is the <u>sheet charge density</u> at that y, times its <u>net drift velocity</u>, times the <u>channel width</u>

MESFET i-v: horizontal drift current problem, cont

We write thus the current as:

$$i_D = -\left[-qN_{ch}(y)\cdot W\cdot \overline{s_y}(y)\right]$$

where -q is the charge per carrier; W is the channel width; and $N_{ch}(y)$ is the sheet carrier density at point y along the channel, which we have already determined by solving the vertical electrostatics problem:

$$N_{ch}(y) \;=\; N_{Dn}\left[a - \sqrt{2\varepsilon_S\left\{\phi_b - \left[v_{GS} - v_{CS}(y)\right]\right\}/qN_{Dn}}\,\right]$$

In the low- to moderate-field region, the average net carrier velocity in the y-direction is the drift velocity:

$$\overline{s_y}(y) = -\mu_e F_y(y) = \mu_e \frac{dv_{CS}(y)}{dy}$$

MESFET i-v: horizontal drift current problem, cont

Putting this all together we get:

$$i_D = -qN_{Dn}\left[a - \sqrt{2\varepsilon_S\left\{\phi_b - \left[v_{GS} - v_{CS}(y)\right]\right\}/qN_{Dn}}\right]\cdot W \cdot \mu_e \frac{dv_{CS}(y)}{dy}$$

We rearrange terms, multiply by dy, and integrate each side from y = 0, v_{CS} = 0, to v = L, v_{CS} = v_{DS}:

$$\int_0^L i_D\, dy = \mu_e q N_{Dn} W \int_0^{v_{DS}} \left[a - \sqrt{\frac{2\varepsilon_S}{qN_{Dn}}}\left(\phi_b - \left[v_{GS} - v_{CS}(y)\right]\right)^{1/2}\right] dv_{CS}$$

Doing the integrals, and dividing both sides by L yields:

$$i_D = a\frac{W}{L} q\mu_e N_{Dn}\left\{v_{DS} - \frac{2}{3}\sqrt{\frac{2\varepsilon_S}{qN_{Dn}a^2}}\left[\left(\phi_b - v_{GS} + v_{DS}\right)^{3/2} - \left(\phi_b - v_{GS}\right)^{3/2}\right]\right\}$$

MESFET i-v: linear or triode region

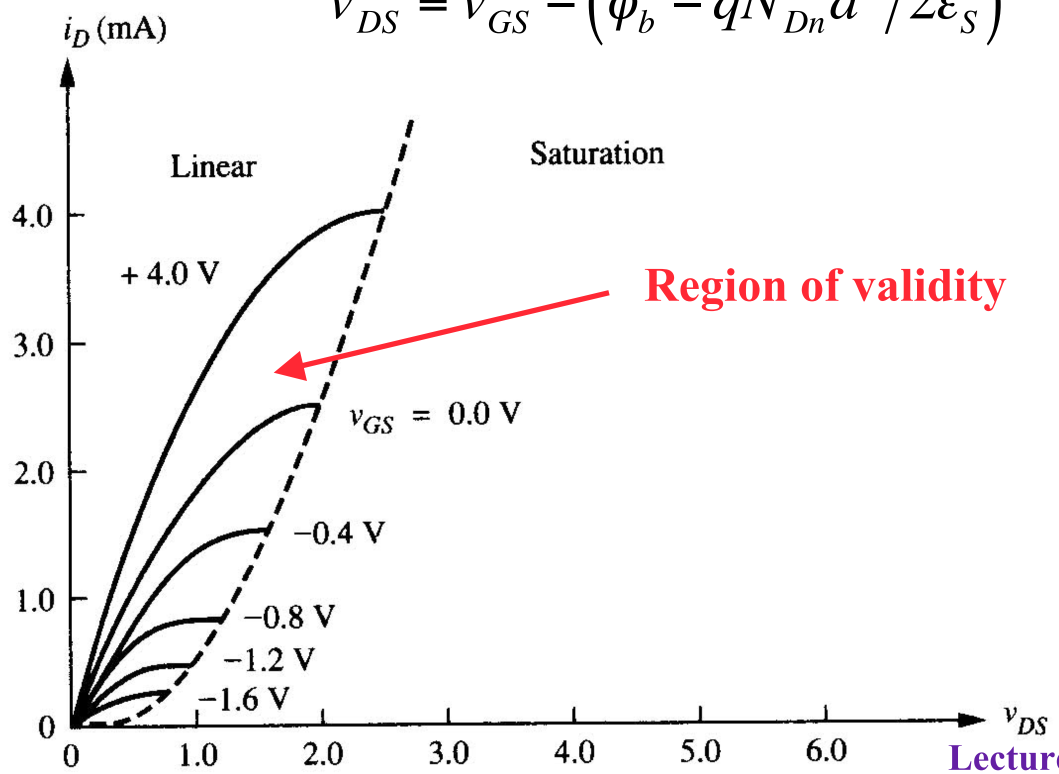
Our result thus far:

$$i_D = a\frac{W}{L}q\mu_e N_{Dn}\left\{v_{DS} - \frac{2}{3}\sqrt{\frac{2\varepsilon_S}{qN_{Dn}a^2}}\left[\left(\phi_b - v_{GS} + v_{DS}\right)^{3/2} - \left(\phi_b - v_{GS}\right)^{3/2}\right]\right\}$$

is only valid until $x_d(y) = a$, which occurs at $y = L$ when

$$v_{DS} = v_{GS} - \left(\phi_b - qN_{Dn}a^2/2\varepsilon_S\right)$$

Plotting this:



MESFET i-v: saturation region

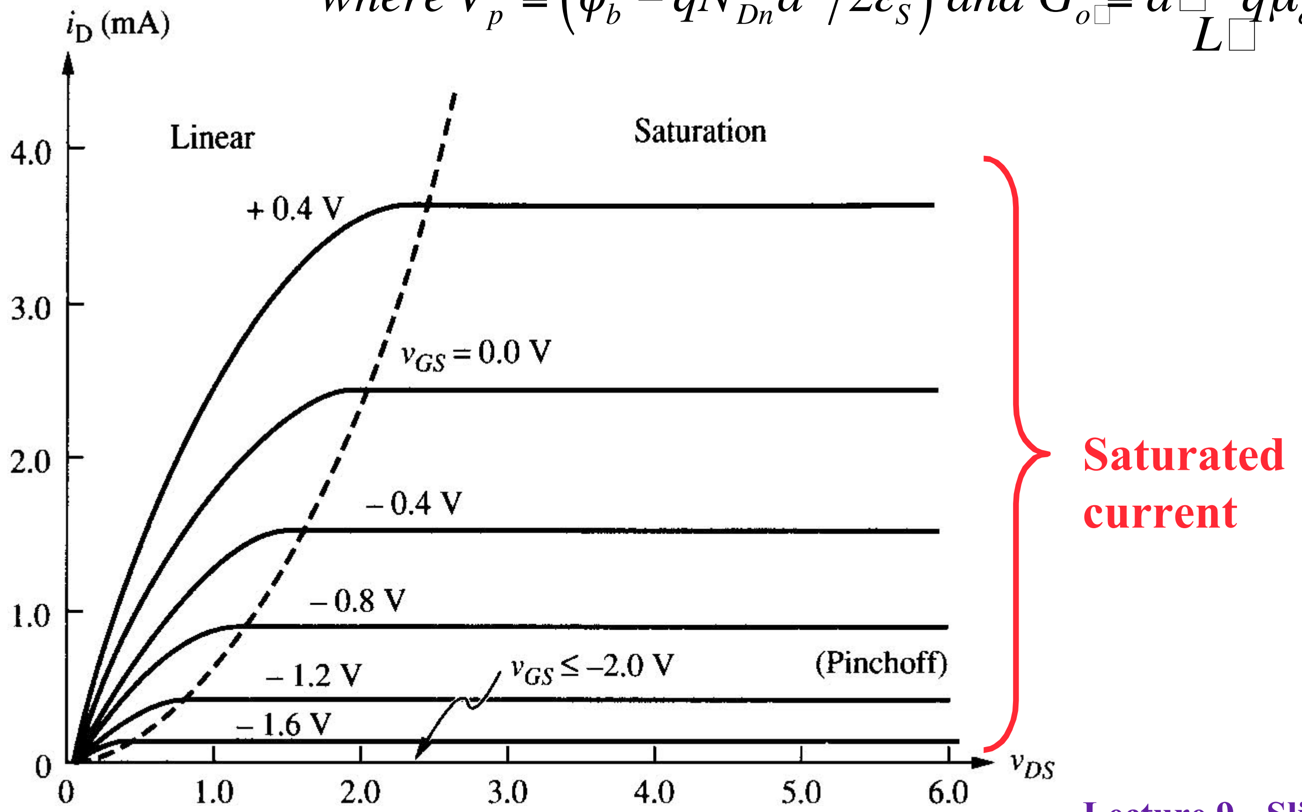
For larger v_{DS}, i.e. when: $v_{DS} > v_{GS} - \left(\phi_b - qN_{Dn}a^2/2\varepsilon_S\right)$

The current, i_D, stays constant at the peak value, which is:

$$i_D = G_o\left\{\left(v_{GS} - V_P\right) - \frac{2}{3}\left[\frac{\left(\phi_b - V_P\right)^{3/2} - \left(\phi_b - v_{GS}\right)^{3/2}}{\left(\phi_b - V_P\right)^{1/2}}\right]\right\},$$

$$where\ V_p \equiv \left(\phi_b - qN_{Dn}a^2/2\varepsilon_S\right)\ and\ G_o \equiv a\frac{W}{L}q\mu_e N_{Dn}$$

Plotting this:



MESFET i-v: summary of characteristics

We identify the pinch-off voltage, V_P, and undepleted channel conductance, G_o:

$$V_p \equiv \left(\phi_b - qN_{Dn}a^2/2\varepsilon_S\right) \qquad G_o \equiv a\frac{W}{L}q\mu_e N_{Dn}$$

We can then write the drain current, i_D, for each of the three regions:

Cutoff:

$$When\ (v_{GS} - V_P) \le 0 \le v_{DS},\ \ i_D = 0$$

When $v_{GS} < V_P$ the channel is pinched off for all v_{DS}, and the device is cut-off,iI.e., $i_D = 0$.

Saturation:

$$When\ 0 \le (v_{GS} - V_P) \le v_{DS},\ i_D = G_o\left\{(v_{GS} - V_P) - \frac{2}{3}\left[\frac{(\phi_b - V_P)^{3/2} - (\phi_b - v_{GS})^{3/2}}{(\phi_b - V_P)^{1/2}}\right]\right\}$$

Linear:

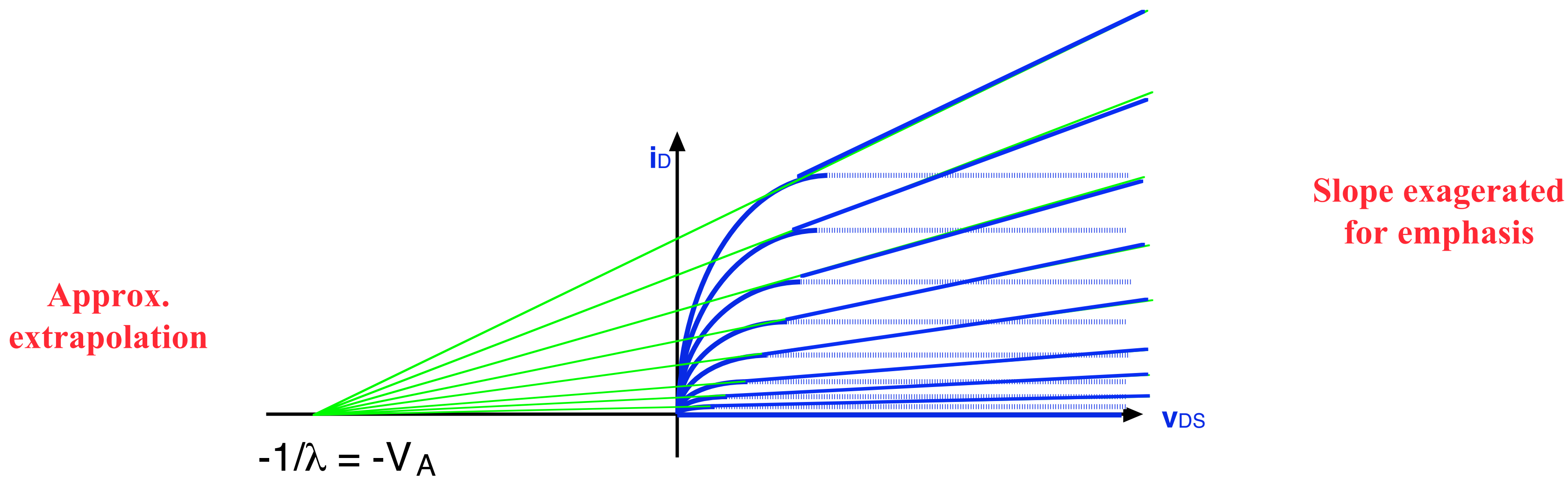
$$When\ 0 \le v_{DS} \le (v_{GS} - V_P),\ i_D = G_o\left\{v_{DS} - \frac{2}{3}\left[\frac{(\phi_b - v_{GS} + v_{DS})^{3/2} - (\phi_b - v_{GS})^{3/2}}{(\phi_b - V_P)^{1/2}}\right]\right\}$$

MESFET characteristics - channel-length modulation

In practice we find that i_D increases slightly with v_{DS} in saturation. This is because the effective channel length decreases with increasing v_{DS} above pinch-off. We model this by saying $L \rightarrow L(1 - \lambda v_{DS})$

$$\text{which means} \quad 1/L \rightarrow (1 + \lambda v_{DS})/L$$

$$\text{and consequently} \quad G_o \rightarrow (1 + \lambda v_{DS})G_o$$



Note: The parameter λ has the units of inverse voltage, and by convention its inverse is called the Early voltage:

$$\text{Early voltage,} \; V_A \equiv 1/\lambda$$

Large signal model: Enhancement mode FETs

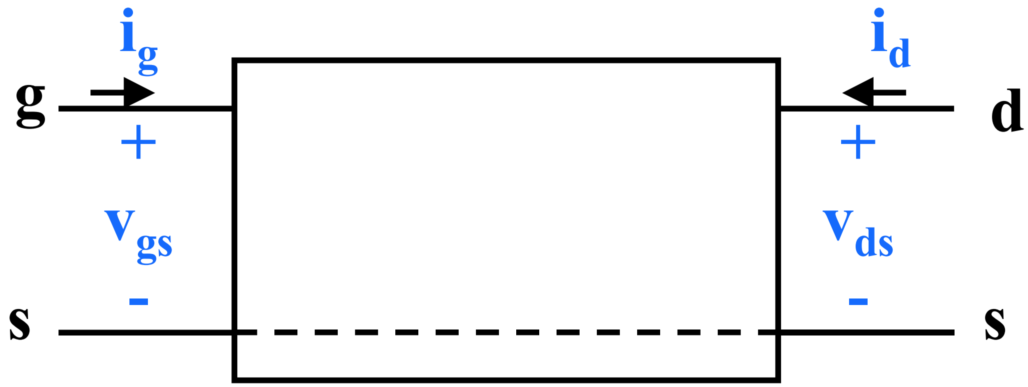
In our discussion thus far we have indicated that there is a conducting channel between the source and drain when the gate is unbiased, I.e., when $v_{GS} = 0$. Such a device is called a "depletion mode" FET.

If the doped layer under the gate is thin enough and/or lightly doped, is possible that the it will be fully depleted when the gate is unbiased. Such a device is called an <u>enhancement mode</u> FET (this is the type of FET most typical of MOSFETs).

The gate of an enhancement mode MESFET must be <u>forward biased</u> to open the channel and turn it on.

Clearly an enhancement mode MESFET can not be turned on very much before the gate diode begins to connect. This is an important limitation, and important difference between MOSFETs and MESFETs.

MESFET - linear equivalent circuit



$$i_g = \left.\frac{\partial i_G}{\partial v_{GS}}\right|_Q v_{gs} + \left.\frac{\partial i_G}{\partial v_{DS}}\right|_Q v_{ds} = g_i v_{gs} + g_r v_{ds}$$

$$i_d = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q v_{gs} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q v_{ds} = g_m v_{gs} + g_o v_{ds}$$

$$g_i \equiv \left.\frac{\partial i_G}{\partial v_{GS}}\right|_Q, \quad g_r \equiv \left.\frac{\partial i_G}{\partial v_{DS}}\right|_Q$$

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q, \quad g_o \equiv \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q$$

MESFET - linear equivalent circuit, cont

The equations on the previous foil are mathematical identities; they tell us nothing about the physics of the device. That comes from using our model to evaluate the derivatives. We want a model to use when the FET is biased in saturation, so we use the current expressions there:

(Remember $i_G = 0$, so g_i and g_r are zero.)

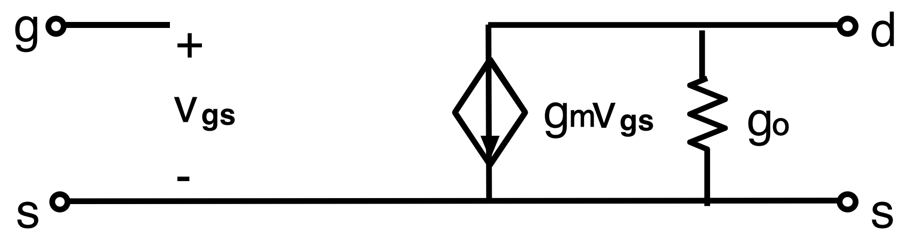
$$g_i \equiv \frac{\partial i_G}{\partial v_{GS}}\Big|_Q = 0 \qquad g_r \equiv \frac{\partial i_G}{\partial v_{DS}}\Big|_Q = 0$$

$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}}\Big|_Q = G_o\left[1 - \sqrt{\frac{(\phi_b - v_{GS})}{(\phi_b - V_P)}}\right]$$

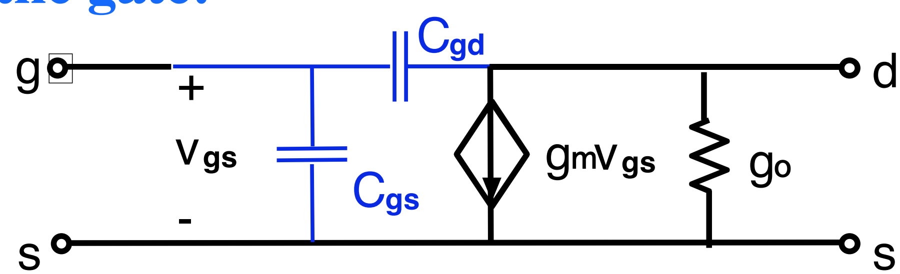
$$g_o \equiv \frac{\partial i_D}{\partial v_{DS}}\Big|_Q \approx \lambda I_D = I_D / V_A$$

Linear equivalent circuit models - schematics

A circuit representation of these results is:



To extend this model to high frequencies we introduce small signal linear capacitors representing the charge stored on the gate:



$$C_{gs} \equiv \left.\frac{\partial q_G}{\partial v_{GS}}\right|_Q \qquad\qquad C_{gd} \equiv \left.\frac{\partial q_G}{\partial v_{DS}}\right|_Q$$

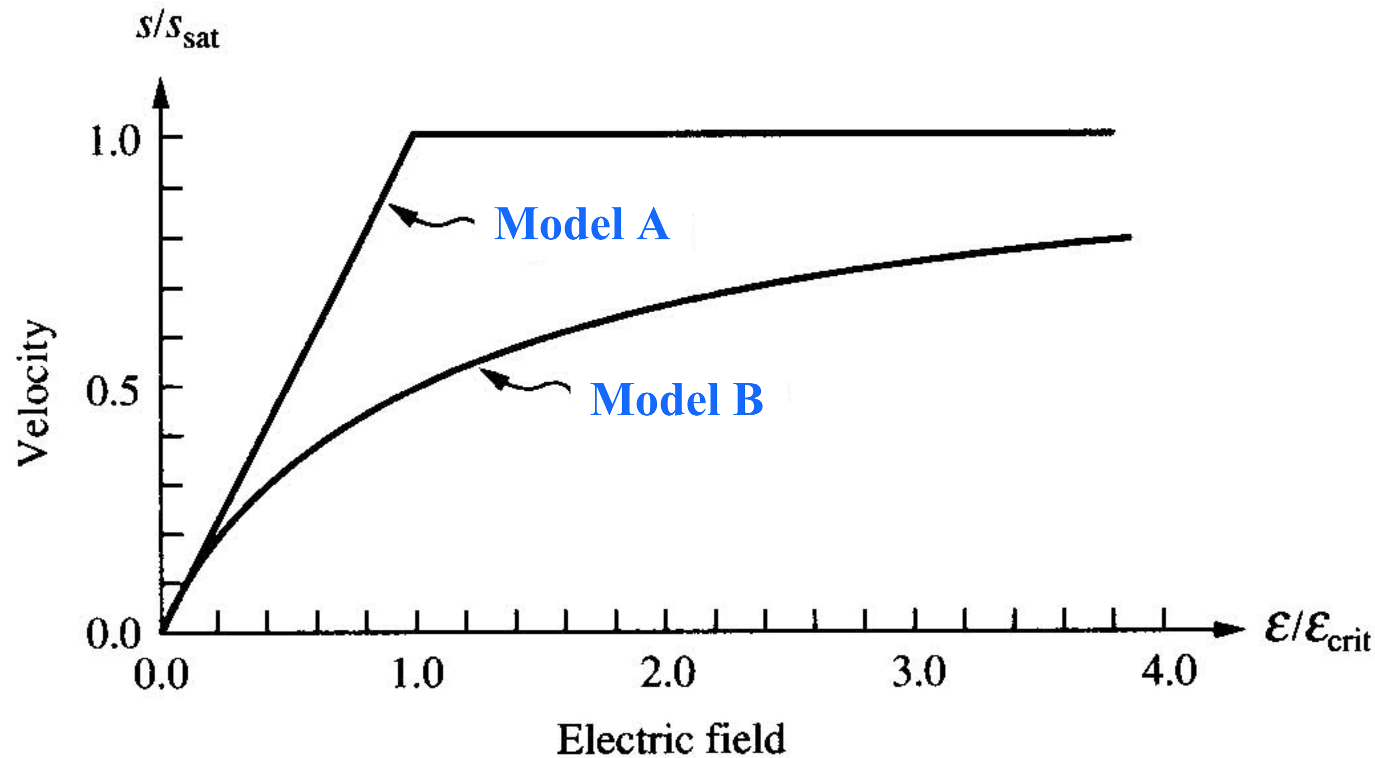
More on this later.

The velocity saturation issue for MESFETs

(Images deleted)

See Fig. 4-10-4: Shur, M. S., Physics of Semiconductor Devices
Englewood Cliffs, N.J.: Prentice-Hall, 1990

Velocity saturation models - impact on MESFET i-v



Model A

$$s_y(F_y) = \mu_e F_y \quad if \quad F_y \leq F_{crit}$$

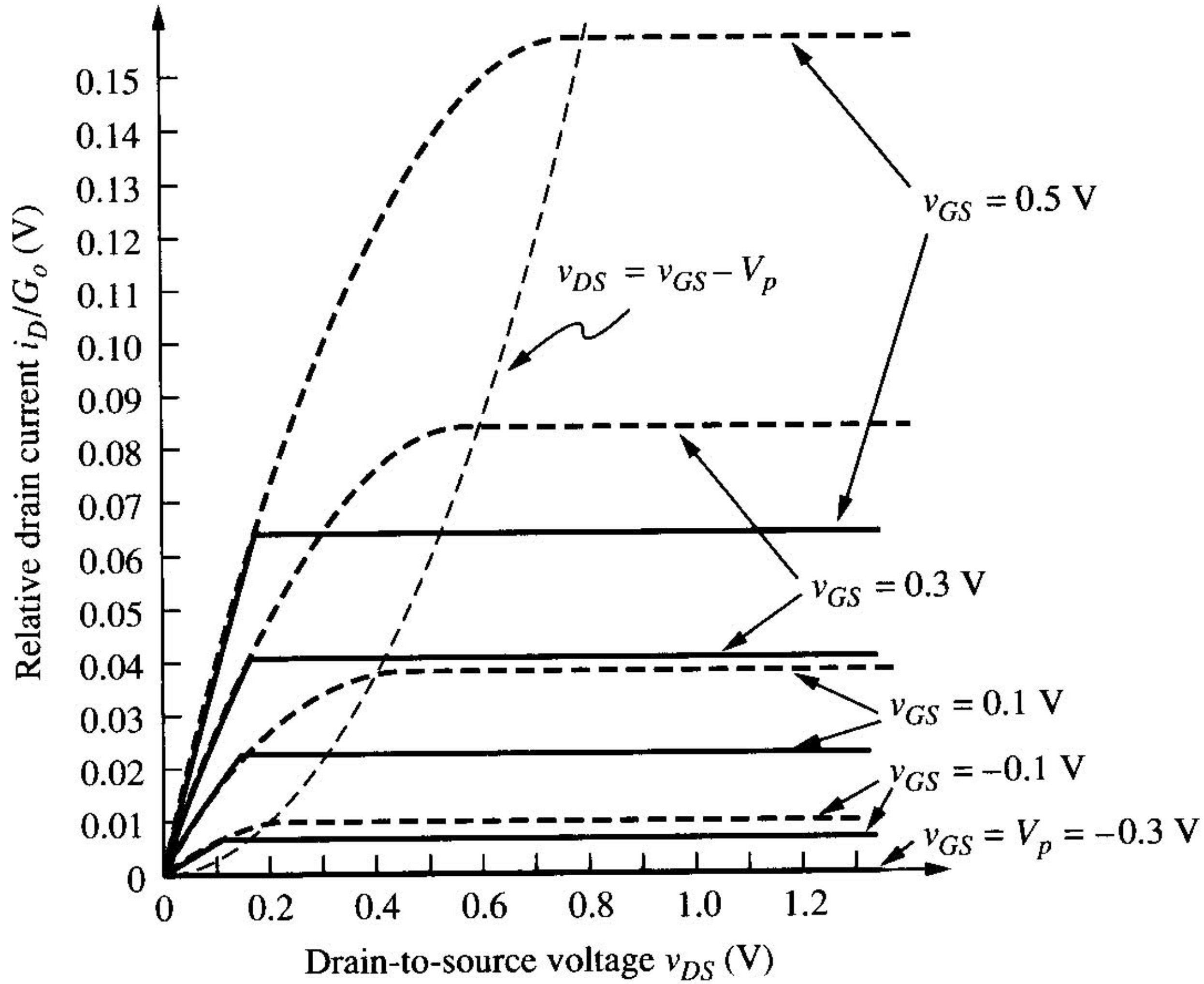
$$= \mu_e F_{crit} \equiv s_{sat} \quad if \quad F_y \geq F_{crit}$$

Model B

$$s_y(F_y) = \frac{\mu_e F_y}{1 + \frac{F_y}{F_{crit}}}$$

Impact of velocity saturation - Model A*

Results of previous modeling hold until s_y at some point equals s_{sat}; after that the current saturates:



* Model A

$$s_y(F_y) = \mu_e F_y \quad if \quad F_y \le F$$

$$= \mu_e F_{crit} \equiv s_{sat} \quad if \quad F_y \ge F_{crit}$$

Impact of velocity saturation - Model B*

Model B

$$s_y(F_y) = \frac{\mu_e F_y}{1 + \dfrac{F_y}{F_{crit}}}$$

It is easy to show that the expression we derived in the linear region with no velocity saturation becomes with this model:

$$i_D = \frac{1}{1 + v_{DS}/F_{crit}L}\, G_o \left\{ v_{DS} - \frac{2}{3}\left[\frac{(\phi_b - v_{GS} + v_{DS})^{3/2} - (\phi_b - v_{GS})^{3/2}}{(\phi_b - V_P)^{1/2}}\right]\right\}$$

$$when\ 0 \leq v_{DS} \leq (v_{GS} - V_P)$$

This is the original expression multiplied by the factor $1/(1+v_{DS}/F_{crit}L)$

High f models and $f_{\backslash}$

A mushroom- or T-gate MESFET

(Image deleted)

See Hollis and Murphy in: Sze, S.M., ed., High Speed Semiconductor Devices
New York: Wiley 1990

Representative processing sequences for MESFETs

Double recess process

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SAINT process

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See Hollis and Murphy in: Sze, S.M., ed., High Speed Semiconductor Devices
New York: Wiley 1990