Lecture 37 - Bipolar Junction Transistor

(cont.)

May 7, 2007

Contents:

1. Common-emitter short-circuit current-gain cut-off frequency, f_T

Reading material:

del Alamo, Ch. 11, §11.4.2

Cite as: Jesús del Alamo, course materials for 6.720J Integrated Microelectronic Devices, Spring 2007.
MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

Key questions

- How is the frequency response of a transistor assessed?
- What determines the frequency response of an ideal BJT?
- How can the frequency response of a BJT be engineered?

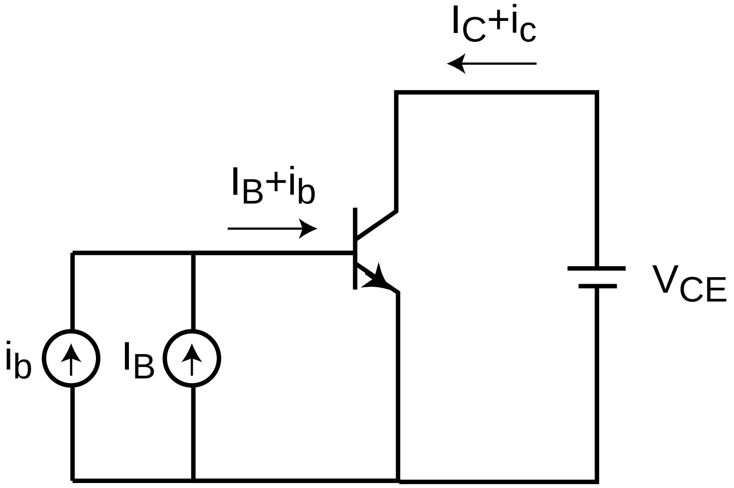
Cite as: Jesús del Alamo, course materials for 6.720J Integrated Microelectronic Devices, Spring 2007.
MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

1. Common-emitter short-circuit current-gain cut-off frequency, f_T

f_T: high-frequency figure of merit for transistors

Short-circuit means from the small-signal point of view.

BJT is biased in FAR.



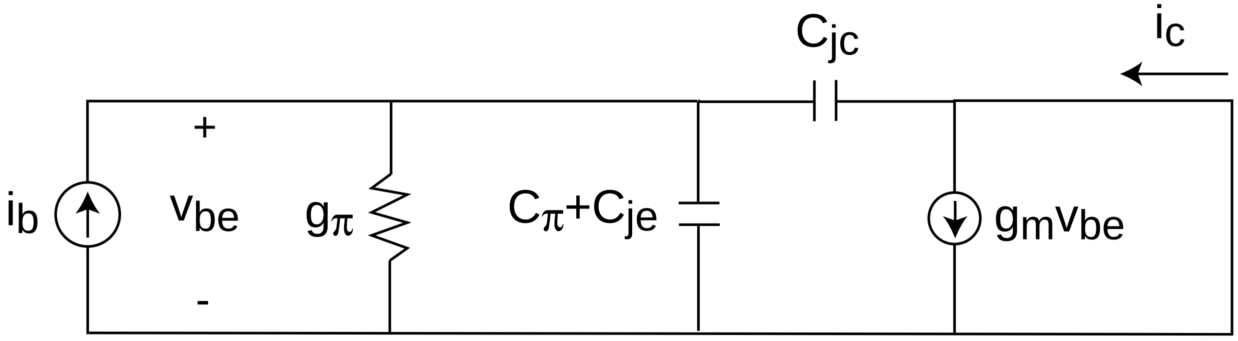
Focus on small-signal current gain:

$$h_{21} = \frac{i_c}{i_b}|_{v_{ce}=0}$$

For low frequency, $h_{21} \rightarrow \beta_F$, for high frequency h_{21} rolls off due to capacitors.

Definition of f_T: frequency at which $|h_{21}| = 1$.

Small-signal equivalent circuit model:



$$
\begin{aligned}
i_c &= g_m v_{be} - j\omega C_{jc} \\
i_b &= [g_\pi + j\omega(C_\pi + C_{je} + C_{jc})]v_{be}
\end{aligned}
$$

Then:

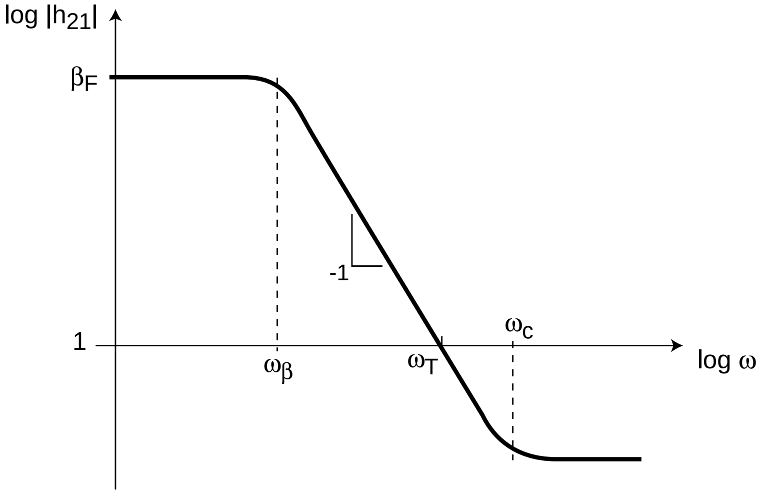
$$h_{21} = \frac{g_m - j\omega C_{jc}}{g_\pi + j\omega(C_\pi + C_{je} + C_{jc})}$$

Magnitude of h_{21}:

$$|h_{21}| = \frac{\sqrt{g_m^2 + \omega^2 C_{jc}^2}}{\sqrt{g_\pi^2 + \omega^2(C_\pi + C_{je} + C_{jc})^2}}$$

$$|h_{21}| = \frac{\sqrt{g_m^2 + \omega^2 C_{jc}^2}}{\sqrt{g_\pi^2 + \omega^2 (C_\pi + C_{je} + C_{jc})^2}}$$

Bode plot of $|h_{21}|$:



Three regimes in $|h_{21}|$:

- low frequency, $\omega \ll \omega_\beta$:

$$|h_{21}| \simeq \frac{g_m}{g_\pi} = \beta_F$$

- intermediate frequency, $\omega_\beta \ll \omega \ll \omega_c$:

$$|h_{21}| \simeq \frac{g_m}{\omega (C_\pi + C_{je} + C_{jc})}$$

- high frequency, $\omega \gg \omega_c$:

$$|h_{21}| \simeq \frac{C_{jc}}{C_\pi + C_{je} + C_{jc}}$$

Angular frequencies that separate three regimes:

$$\omega_\beta = \frac{g_\pi}{C_\pi + C_{je} + C_{jc}}$$

$$\omega_c = \frac{g_m}{C_{jc}}$$

Angular frequency at which $|h_{21}| = 1$:

$$\omega_T = \frac{g_m}{C_\pi + C_{je} + C_{jc}}$$

In terms of frequency:

$$f_T = \frac{g_m}{2\pi(C_\pi + C_{je} + C_{jc})}$$

Note:

$$\omega_\beta = \frac{\omega_T}{\beta_F}$$

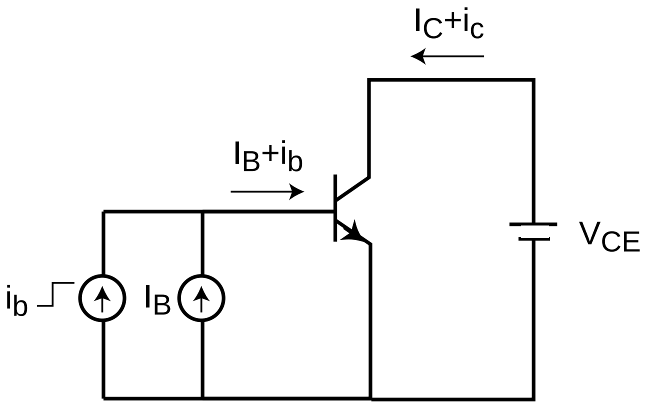
□ Physical meaning of f_T

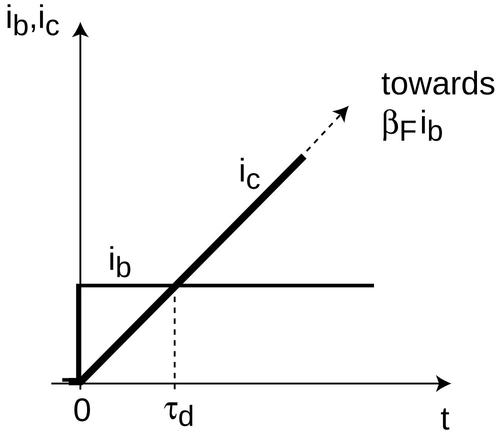
$1/2\pi f_T$ has units of time. Define *delay time*:

$$\tau_d = \frac{1}{2\pi f_T} = \frac{C_\pi}{g_m} + \frac{C_{je}}{g_m} + \frac{C_{jc}}{g_m} = \tau_{tB} + \frac{\tau_{tE}}{\beta_F} + \frac{C_{je}}{g_m} + \frac{C_{jc}}{g_m}$$

Four delay components in τ_d.

Consider response of BJT to a step-input base current:





At $t = 0$

$$I_B \rightarrow I_B + i_b$$

As $t \rightarrow \infty$

$$V_{BE} \rightarrow V_{BE} + v_{be}$$

$$I_C \rightarrow I_C + i_c = I_C + \beta_F i_b.$$

Cite as: Jesús del Alamo, course materials for 6.720J Integrated Microelectronic Devices, Spring 2007.
MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].

How much time does it take for i_C to reach its final value?

Charge must be delivered to four regions in BJT:

- *Quasi-neutral emitter*

$$q_e = \tau_{tE} i_b$$

- *Quasi-neutral base*

$$q_b = \tau_{tB} i_c$$

- *Emitter-base depletion region*

$$q_{je} = C_{je} v_{be} = \frac{C_{je}}{g_m} i_c$$

- *Base-collector depletion region*

$$q_{jc} = C_{jc} v_{bc} = C_{jc} v_{be} = \frac{C_{jc}}{g_m} i_c$$

Charge delivered at constant rate to base. Time that it takes for all charge to be delivered:

$$\tau_\beta = \frac{q_e + q_b + q_{je} + q_{jc}}{i_b} = \tau_{tE} + \beta_F(\tau_{tB} + \frac{C_{je}}{g_m} + \frac{C_{jc}}{g_m}) = \frac{1}{2\pi f_\beta}$$

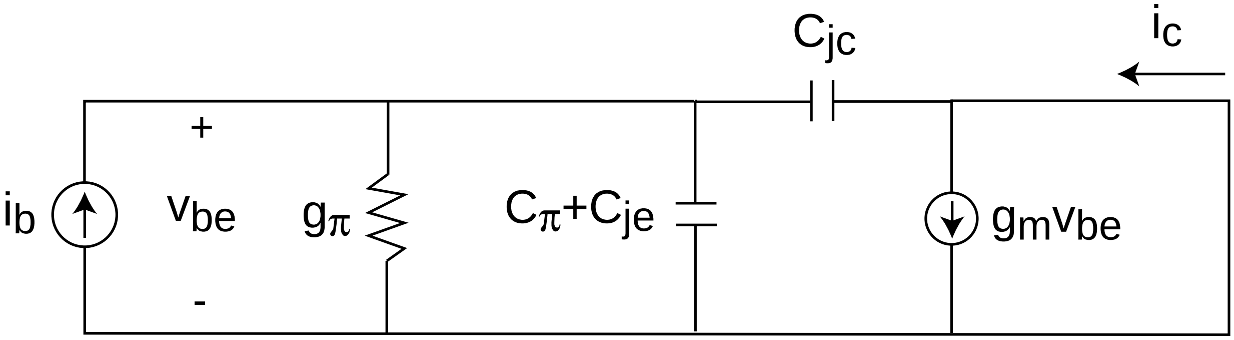
How much time does it take for i_C to build up to $I_C + i_b$?

Since $i_c = \beta_F i_b$,

$$\tau_d = \frac{\tau_\beta}{\beta_F} = \frac{\tau_{tE}}{\beta_F} + \tau_{tB} + \frac{C_{je}}{g_m} + \frac{C_{jc}}{g_m} = \frac{1}{2\pi f_T}$$

- $\tau_d = \frac{1}{2\pi f_T}$: delay time before i_C increases to $I_C + i_b$
- $\tau_\beta = \frac{1}{2\pi f_\beta}$: delay time before i_C increases to $I_C + \beta_F i_b$

With sinusoidal input:



$f \uparrow \Rightarrow$ fraction of i_b that goes into capacitors$\uparrow \Rightarrow v_{be} \downarrow \Rightarrow i_c \downarrow$.

At f_T : $|i_c| = |i_b|$

□ Key dependencies of f_T in ideal BJT

⋆ f_T dependence on I_C:

Rewrite f_T:

$$f_T = \frac{g_m}{2\pi(C_\pi + C_{je} + C_{jc})} = \frac{1}{2\pi\tau_F}\frac{1}{1 + \frac{kT}{q\tau_F}\frac{C_{je}+C_{jc}}{I_C}}$$

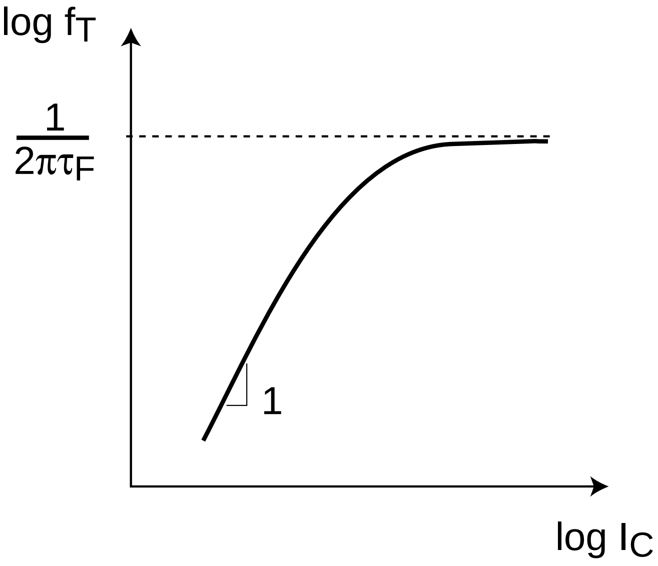
Two limits:

- Small I_C: limited by depletion capacitances

$$f_T \simeq \frac{q}{2\pi kT}\frac{I_C}{C_{je} + C_{jc}}$$

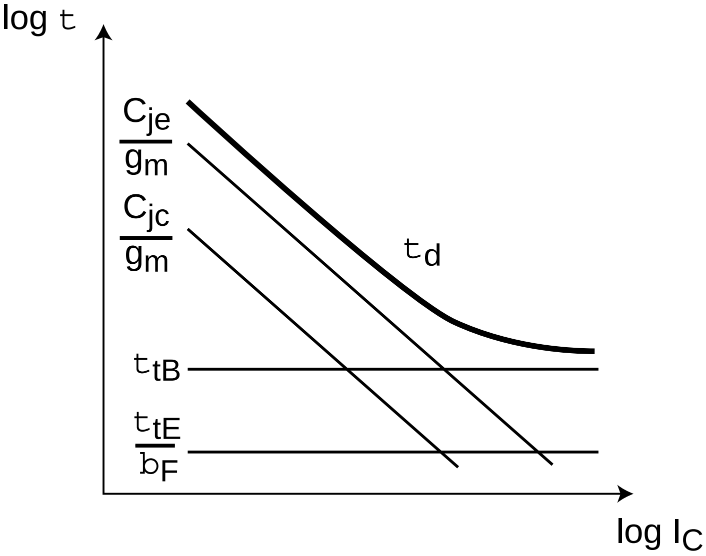
- Large I_C: limited by intrinsic delay (dominated by τ_{tB})

$$f_T \simeq \frac{1}{2\pi\tau_F}$$

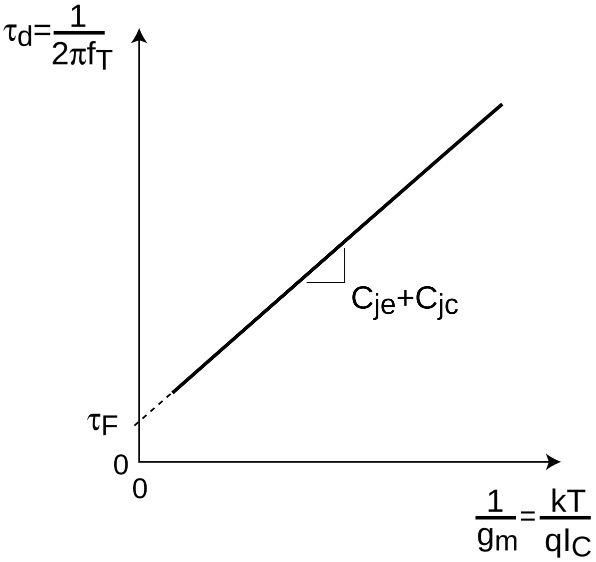


Alternative view of I_C dependence:

$$\tau_d = \frac{\tau_{tE}}{\beta_F} + \tau_{tB} + \frac{C_{je}}{g_m} + \frac{C_{jc}}{g_m} = \frac{1}{2\pi f_T}$$



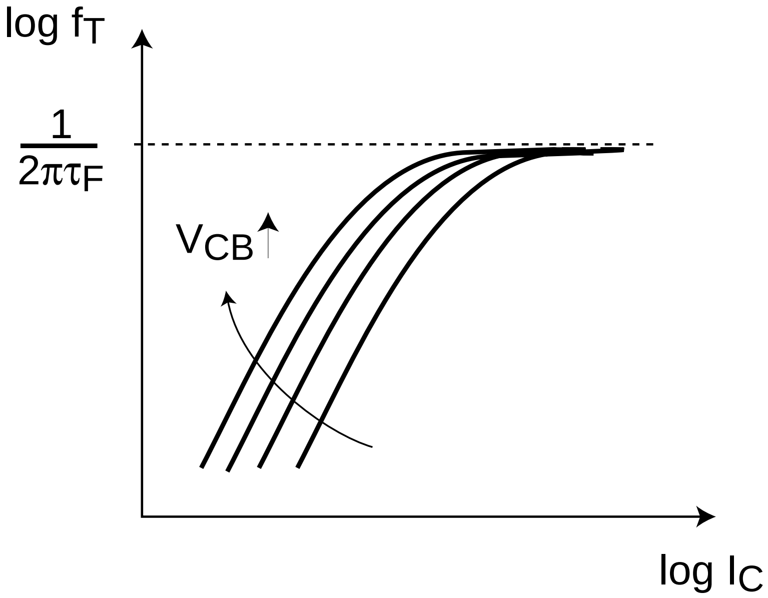
Standard experimental technique to extract τ_F and $C_{je} + C_{jc}$:



$\star$ f_T dependence on V_{BC}:

$V_{CB}\uparrow$ (B-C junction is more reverse biased) $\Rightarrow C_{jc}\downarrow\ \Rightarrow f_T\uparrow$

[but only in low I_C regime of f_T]



$\star$ f_T dependence on device layout:

- For low I_C: f_T dominated by $C_{je},\ C_{jc}$

$$\frac{C_{je}}{g_m} \propto \frac{A_E C_{jeo}}{I_C}$$

$$\frac{C_{jc}}{g_m} \propto \frac{A_C C_{jco}}{I_C}$$

If $A_E\uparrow$ or $A_C\uparrow$ (keeping I_C constant) $\Rightarrow f_T\downarrow$

- For high I_C: f_T dominated by τ_F; f_T independent of A_E or A_C

□ Device design strategies for improving f_T

Four delay terms in f_T:

$$\tau_d = \frac{1}{2\pi f_T} = \frac{\tau_{tE}}{\beta_F} + \tau_{tB} + \frac{C_{je}}{g_m} + \frac{C_{jc}}{g_m}$$

Strategies to reduce each delay component:

⋆ *Emitter charging time*, $\frac{\tau_{tE}}{\beta_F}$, minimized by

- enhancing β_F,
- having a shallow emitter ($\tau_{tE} \sim W_E^2$),
- building steep doping profile in emitter.

$\frac{\tau_{tE}}{\beta_F}$ small contribution to τ_d, not much payoff.

⋆ *Base transit time*, τ_{tB}, minimized by

- reducing W_B ($\tau_{tB} \sim W_B^2$),
- introducing drift field in base (through impurity gradient or SiGe composition gradient).

Significant device engineering towards minimizing τ_{tB}.

Example 1 [Kasper 1993]:

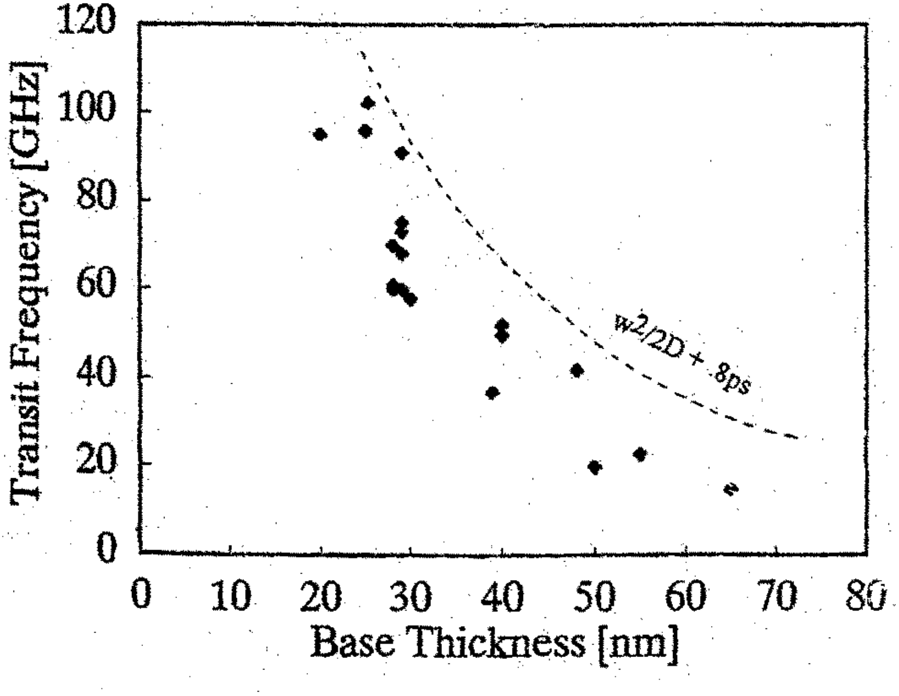


Fig. 2: Transit frequency f_T versus SiGe thickness (effective base width)

[Kasper, 1993]

Kasper, E., and A. Gruhle. "Silicon Germanium Heterobipolar Transistor for High Speed Operation." *Proceedings of the IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, August 2-4, 1993*. New York, NY: IEEE Electron Devices Society, 1993, pp. 23-30. ISBN: 9780780308954. Copyright 1993 IEEE. Used with permission.

Example 2 [Yamazaki, IEDM 1990, p. 309]:

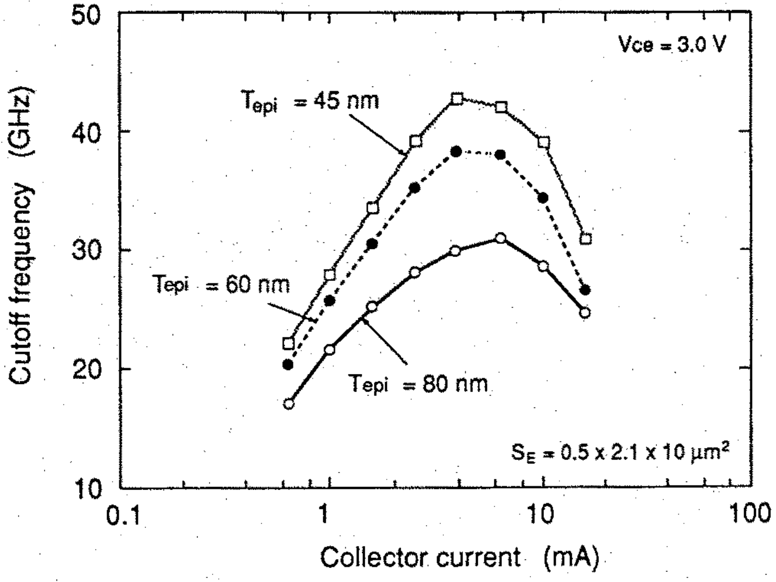


Fig. 5 Cutoff frequency as a function of collector current.

Yamazaki, T., et al. "A 11.7 GHz 1/8-divider Using 43 GHz Si High Speed Bipolar Transistor with Photoepitaxially Grown Ultra-thin Base." *Technical Digest of the International Electron Devices Meeting, San Francisco, CA, December 9-12, 1990.* New York, NY: Institute of Electrical and Electronics Engineers, 1990, pp. 309-312. Copyright 1990 IEEE. Used with permission.

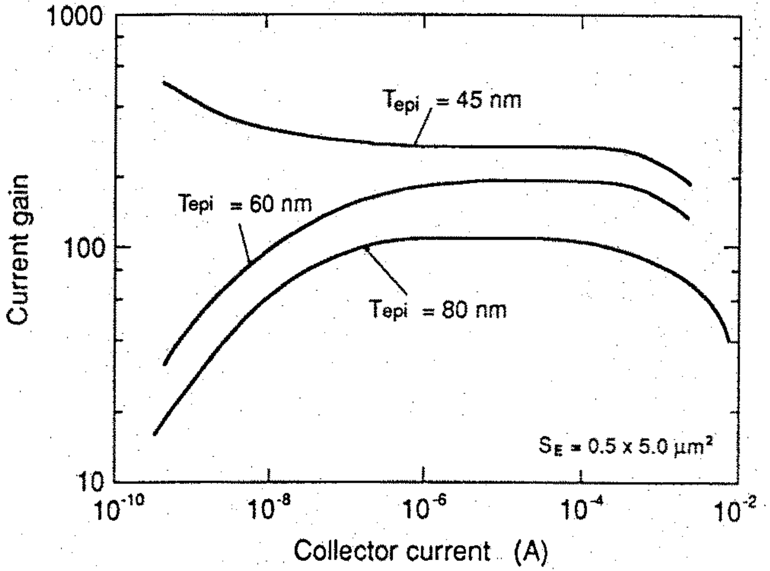


Fig. 4 Current gain versus collector current characteristics.

Yamazaki, T., et al. "A 11.7 GHz 1/8-divider Using 43 GHz Si High Speed Bipolar Transistor with Photoepitaxially Grown Ultra-thin Base." *Technical Digest of the International Electron Devices Meeting, San Francisco, CA, December 9-12, 1990.* New York, NY: Institute of Electrical and Electronics Engineers, 1990, pp. 309-312. Copyright 1990 IEEE. Used with permission.

Example 3 [Crabbé, IEDM 1990, p. 17]:

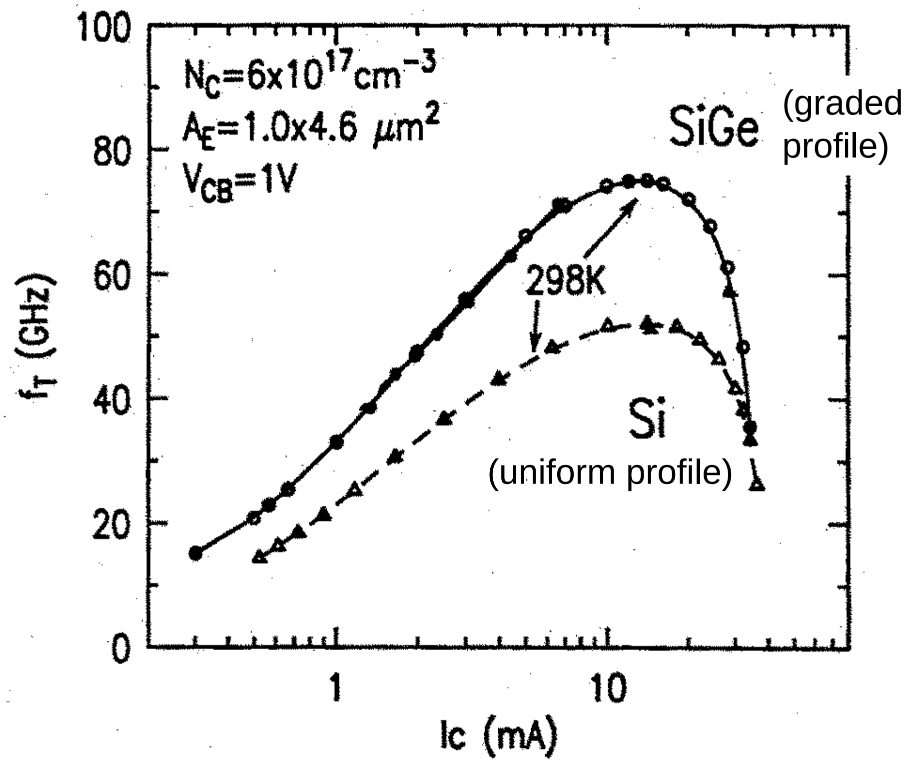


Fig. 10. Collector current dependence of f_T at 298K and 85K for Si and SiGe devices. In both cases, the peak f_T increases at lower temperature as well as the associated collector current.

Crabbe, E. F., et. al. "Low Temperature Operation of Si and SiGe Bipolar Transistors." *Technical Digest of the International Electron Devices Meeting, San Francisco, CA, December 9-12, 1990.* New York, NY: Institute of Electrical and Electronics Engineers, 1990, pp. 17-20. Copyright 1990 IEEE. Used with permission.

⋆ *E-B SCR charging time*, C_{je}/g_m:

$$\frac{C_{je}}{g_m} \propto \frac{A_E C_{jeo}}{I_C} = \frac{C_{jeo}}{J_C}$$

Minimized by:

- $N_B \downarrow$
- tailoring doping profiles at E-B junction

⋆ *B-C SCR charging time*, C_{jc}/g_m:

$$\frac{C_{jc}}{g_m} \propto \frac{A_C C_{jco}}{I_C} = \frac{A_C}{A_E}\frac{C_{jco}}{J_C}$$

Minimized by:

- $N_C \downarrow$
- tailoring doping profiles at B-C junction.
- tightening layout of transistor: $\frac{A_C}{A_E} \rightarrow 1$

Key conclusions

- f_T: high-frequency figure of merit for transistors: frequency at which $|h_{21}| = 1$.
- f_T of ideal BJT:

$$f_T = \frac{g_m}{2\pi(C_\pi + C_{je} + C_{jc})}$$

- *Delay time*, $\tau_d = \frac{1}{2\pi f_T}$: time it takes for step increase in i_B to yield an identical step increase in i_C.
- Most effective ways to engineer f_T:
  - reduce W_B
  - introduce drift field in base (through impurity gradient or SiGe composition gradient)
  - tighten layout: $\frac{A_C}{A_E} \rightarrow 1$