Lecture 15 - p-n Junction *(cont.)*

March 9, 2007

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1. Ideal p-n junction out of equilibrium (cont.)
2. pn junction diode: parasitics, dynamics

Reading assignment:

del Alamo, Ch. 6, §6.2 (6.2.4), §6.3

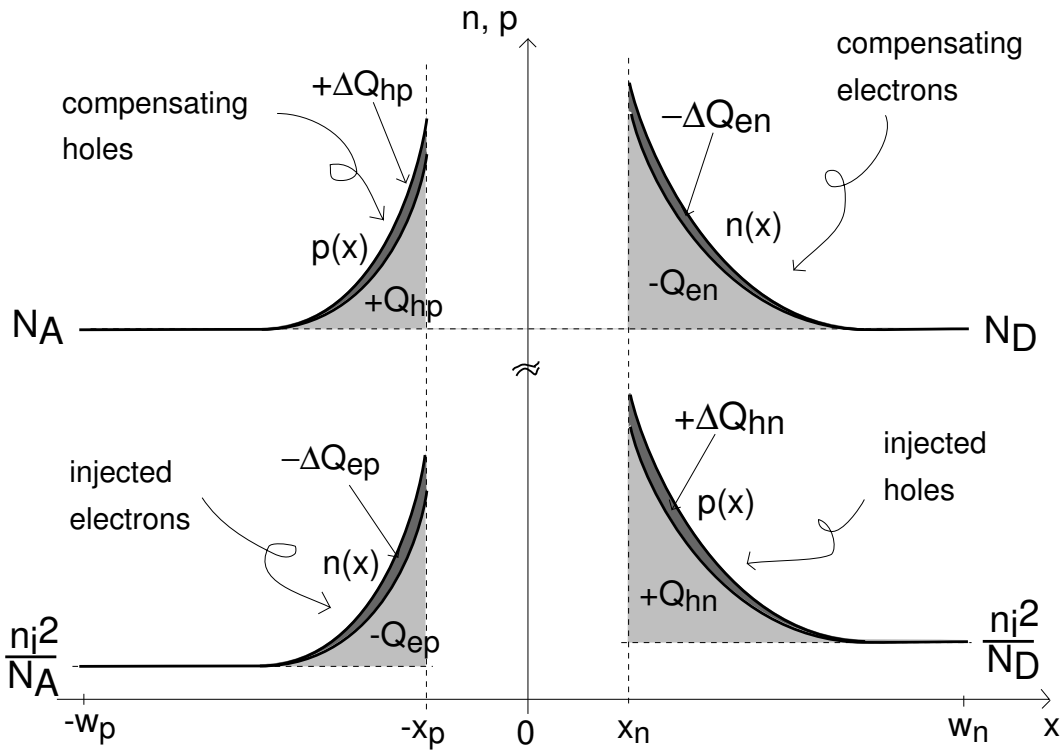
Key questions

- What happens to the *majority carriers* in a pn junction under bias?
- What are the main practical issues in synthesizing pn junction diodes?
- How does a pn junction switch? What dominates its dynamic behavior?

1. Ideal p-n junction out of equilibrium *(cont.)*

□ Minority carrier storage

Quasi-neutrality in QNR's demands $n' \simeq p'$. Consequences:



In n-QNR, quasi-neutrality implies:

$$Q_{hn} \simeq |Q_{en}| \equiv Q_n$$

Also, if $V \uparrow \rightarrow Q_{hn} \uparrow \rightarrow |Q_{en}| \uparrow$ with:

$$\Delta Q_{hn} \simeq |\Delta Q_{en}| \equiv \Delta Q_n$$

ΔQ_{hn} supplied from p-contact, ΔQ_{en} supplied from n-contact.

Looks like a capacitor ⇒ **diffusion capacitance**.

Diffusion capacitance (per unit area):

$$C_d = \frac{dQ_n}{dV} + \frac{dQ_p}{dV}$$

with:

$$Q_n = q\int_{x_n}^{w_n} p'(x)dx$$

$$Q_p = q\int_{-w_p}^{-x_p} n'(x)dx$$

• If both sides are "long":

$$Q_n = qL_h p'(x_n) = \tau_h J_h(x_n)$$
$$Q_p = qL_e n'(-x_p) = \tau_e J_e(-x_p)$$

and

$$C_d \simeq \frac{q}{kT}[\tau_h J_h(x_n) + \tau_e J_e(-x_p)] = \frac{q}{kT}(\tau_h J_{hs} + \tau_e J_{es}) \exp\frac{qV}{kT}$$

• If both sides are short and $S = \infty$:

$$Q_n = q\frac{1}{2}p'(x_n)(w_n - x_n) = \tau_{tn}J_h(x_n)$$
$$Q_p = q\frac{1}{2}n'(-x_p)(w_p - x_p) = \tau_{tp}J_e(-x_p)$$

with τ_{tn} and τ_{tp} are the minority carrier transit times through QNR's:

$$\tau_{tn} = \frac{(w_n - x_n)^2}{2D_h}$$
$$\tau_{tp} = \frac{(w_p - x_p)^2}{2D_e}$$

Then:

$$C_d \simeq \frac{q}{kT}[\tau_{tn}J_h(x_n) + \tau_{tp}J_e(-x_p)] = \frac{q}{kT}(\tau_{tn}J_{hs} + \tau_{tp}J_{es})\exp\frac{qV}{kT}$$

Similar result to long diode!

- General expression:

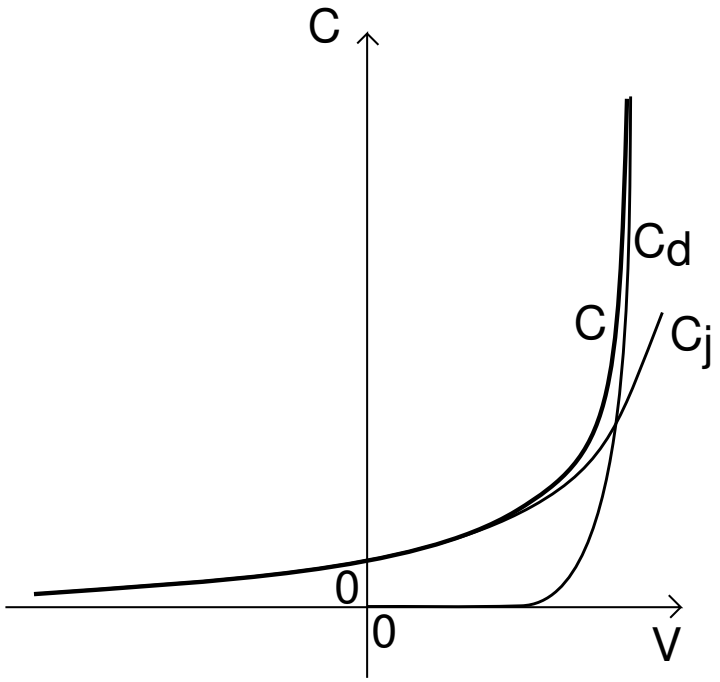
$C_d = \frac{q}{kT}\Sigma_{n,p}$ dominant minority carrier time constant
$\times$injected minority carrier current density

C_d grows exponentially in forward bias, negligible in reverse bias:

$$C_d \sim \exp\frac{qV}{kT}$$

[check that $C_d \sim \exp\frac{qV}{kT}$ and not $\sim \exp\frac{qV}{kT} - 1$]

- Total diode capacitance:



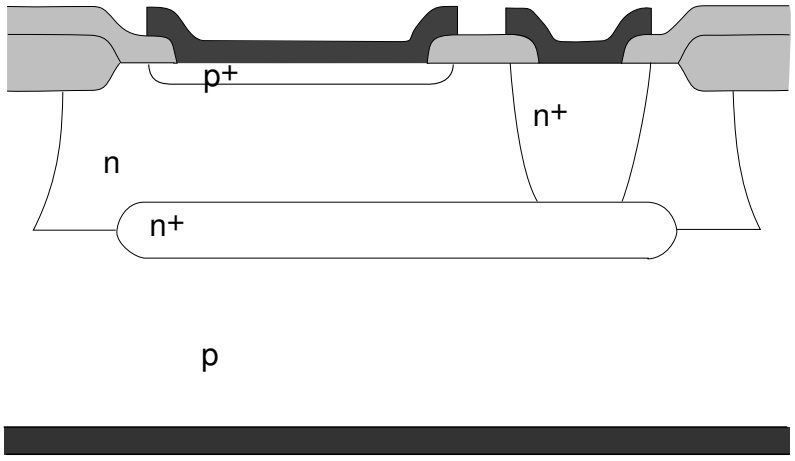
2. p-n junction diode

• pn junctions present in most semiconductor devices (BJTs and MOSFETs).

• pn junction diodes used in rectifying circuits, detectors in communications applications, bias shifters, input protection devices against electrostatic discharge.

• For integrated p-n diodes, no special process steps available.

Typical cross section of p-n diode implemented in BJT process:

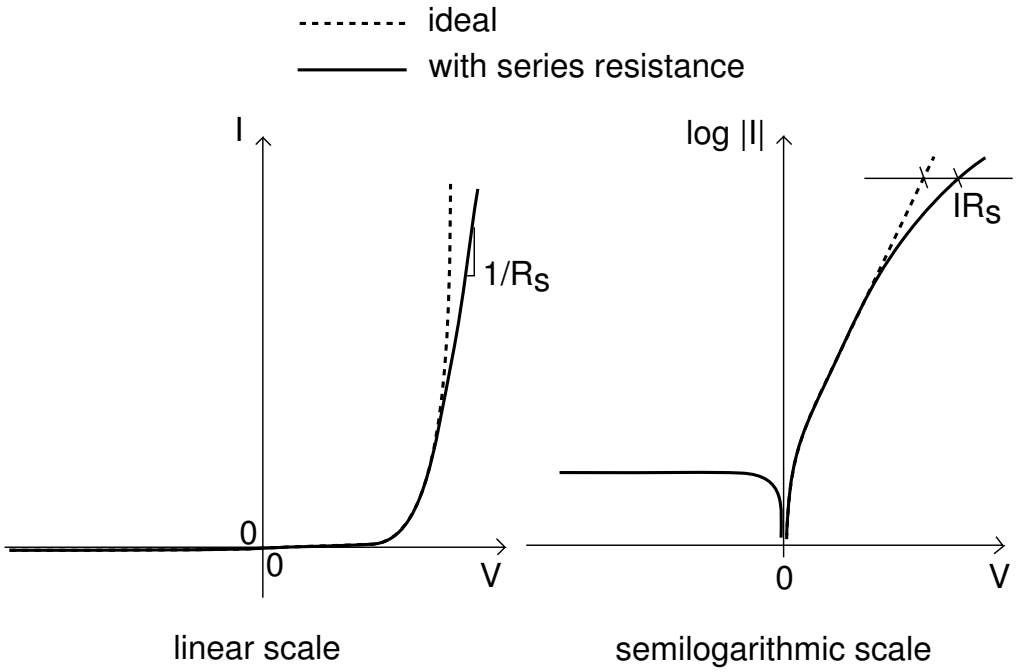


□ Parasitics

⋆ *Series resistance:*

- Accounts for ohmic drop in QNR's (neglected so far).
- Reduces internal diode voltage $\rightarrow I \downarrow$

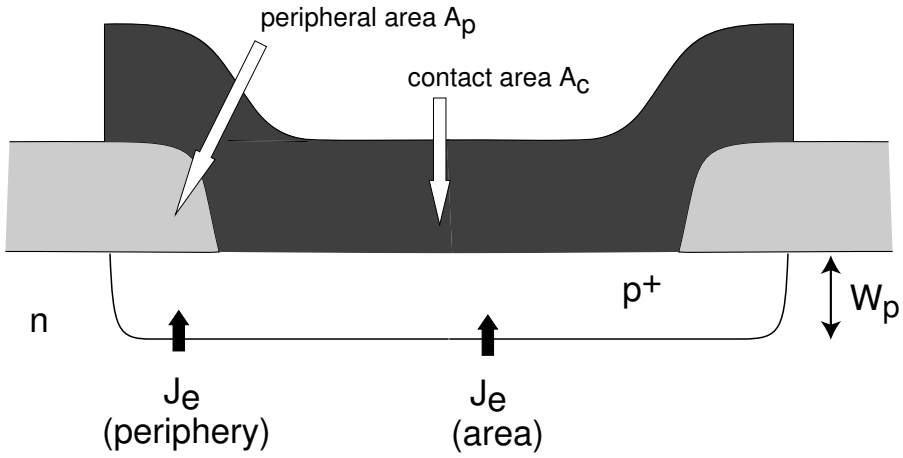
$$I = I_s[\exp \frac{q(V - IR_s)}{kT} - 1]$$



- Higher V_F required to deliver desired $I_F \rightarrow$ more power dissipation, potential process control problems
- RC time constant degraded.

⋆ *Minority carrier boundary conditions*:

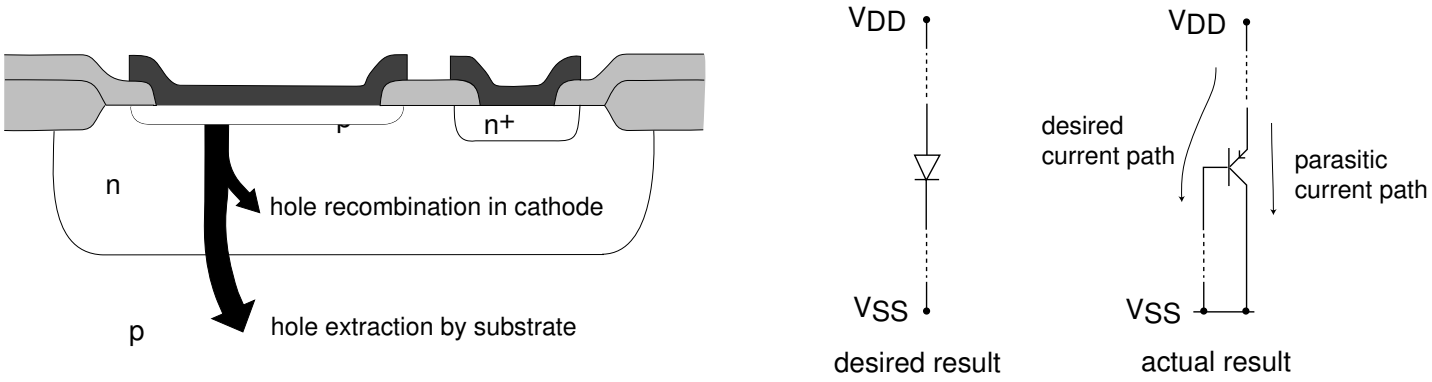
- At top surface: depending on relative depth of emitter, effective diode area changes
  - top surface=ohmic contact area (A_c, $S = \infty$)
    + peripheral SiO_2-covered area (A_p, $S = 0$)



  - if $W_p \gg L_e$, volume recombination only $\rightarrow A_{eff} \simeq A_c + A_p$
  - if $W_p \ll L_e$, surface recombination only $\rightarrow A_{eff} \simeq A_c$
- At bottom surface: high-low junction, characterized by S_{hl}.

⋆ *Isolation*:

- Parasitic substrate p-n junction → needs to be reverse biased to avoid turning it on.
- Even reverse biased, substrate contributes parasitic capacitance.
- Additional danger: "bipolar effect" between diode and substrate → minority carriers can be extracted by substrate → current diverted away from main body of diode.

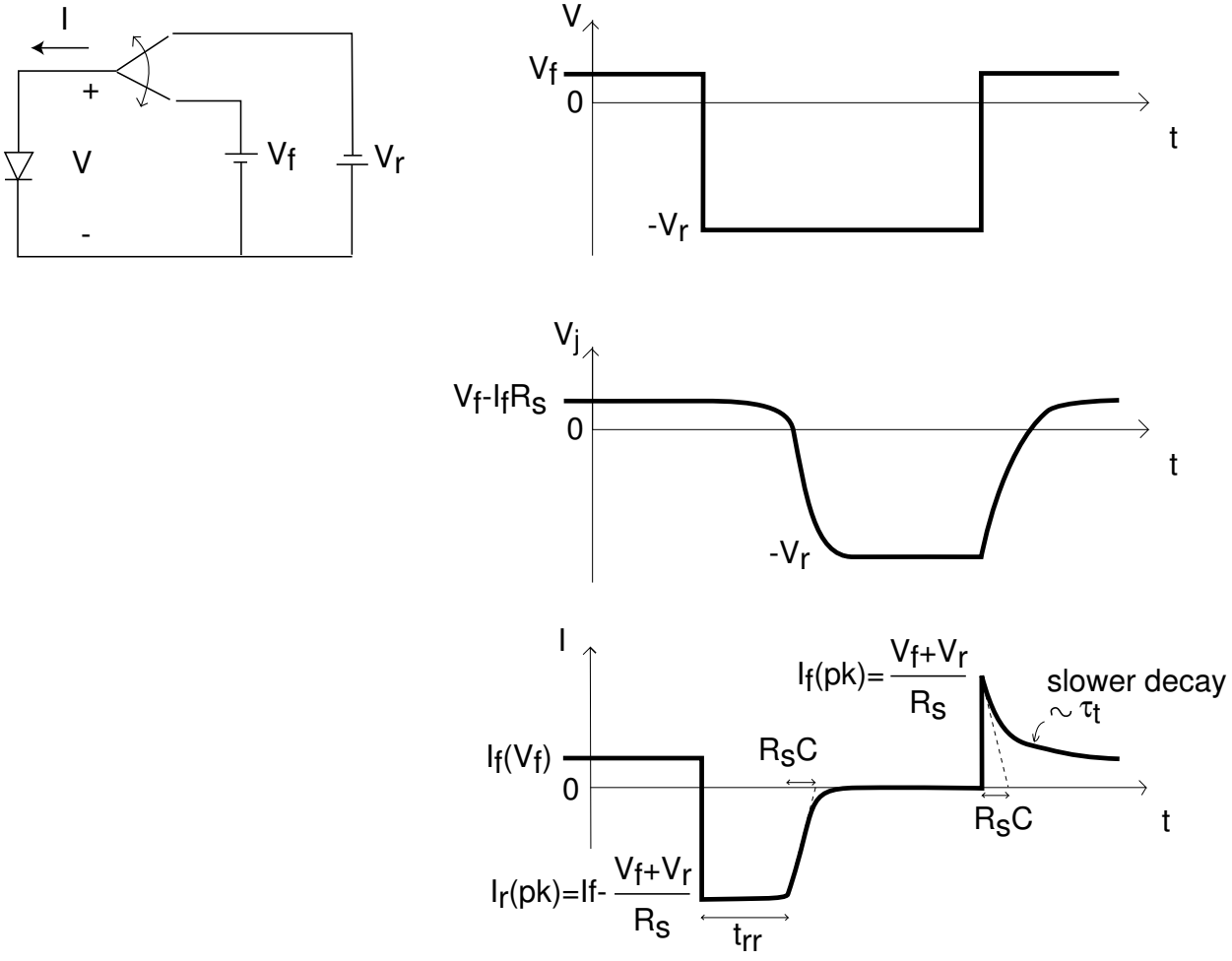


- Hard to make integrated pn diodes in CMOS process (unless they hang directly from the power rail that is connected to the substrate).
- Easier in bipolar since n^+ buried layer and collector plug can prevent minority carrier injection.

□ Dynamics

Fundamental difference between p-n and Schottky diodes: minority carrier storage slows down p-n diode.

Consider simple voltage switching:

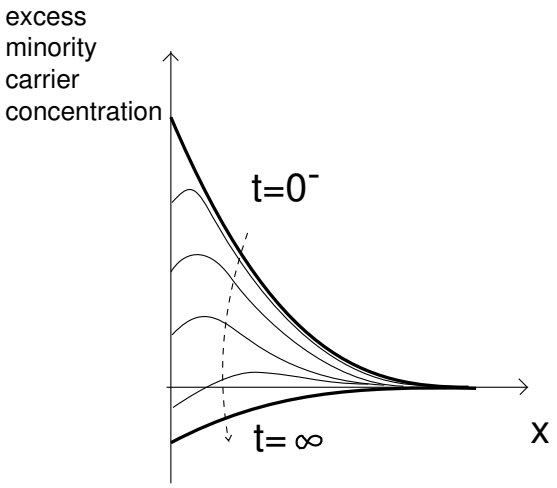


As in Schottky diode, delays associated with $R_s C_j$.

Additionally, delays associated with minority carrier storage.

⋆ Switch-off transient

Evolution of excess minority carrier concentration (long diode):



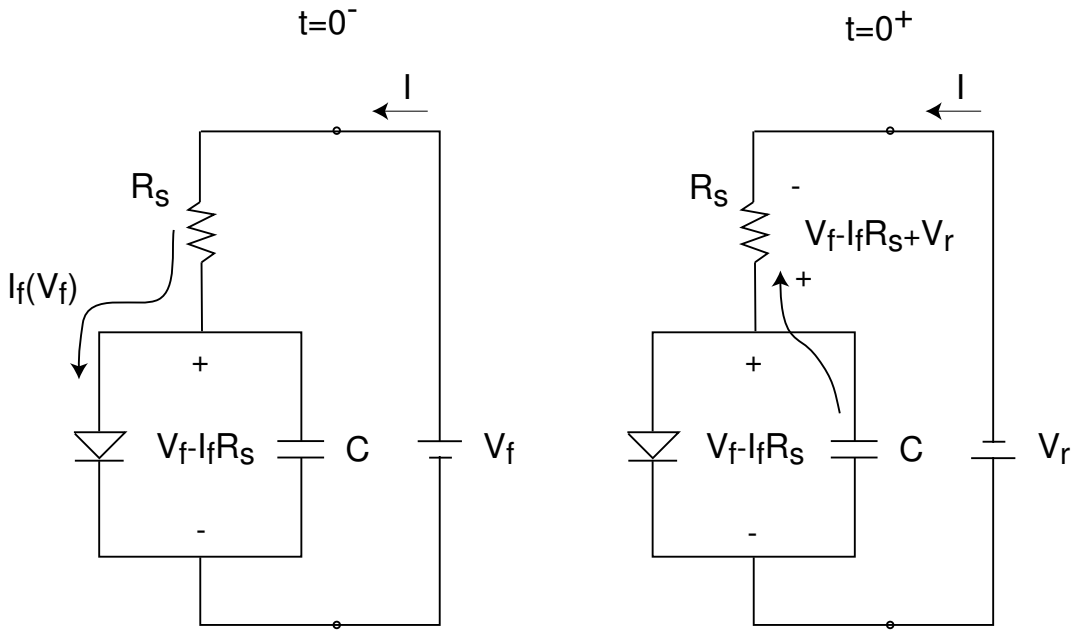
switch-off

At $t = 0^-$, $V_f \rightarrow I_f$; minority carrier stored charge:

$$Q = \tau_t I_f$$

with τ_t, dominant minority carrier time constant.

At $t = 0^+$, external V abruptly changes from V_f to V_r; internal V cannot change abruptly $\rightarrow$ need to get rid of minority carriers!



$$I(0^-) = I_f(V_f) \qquad I(0^+) = -\frac{1}{R_s}(V_f - I_f R_s + V_r) \simeq -\frac{V_r}{R_s}$$

Two phases to discharge:

Phase I - From $V_j = V_f - I_f R_s$ to $V_j \simeq 0$.

Since $Q \sim \exp \frac{qV_f}{kT}$, as Q discharges, V_f cannot change much.

Discharge proceeds nearly at constant current $I_r(pk) \simeq -\frac{V_r}{R_s}$

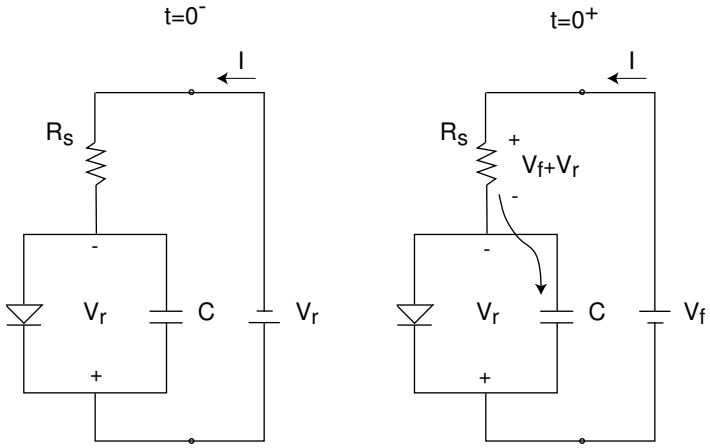
Time to discharge (*reverse recovery time*):

$$t_{rr} \simeq \frac{Q}{|I_r(pk)|} \simeq \tau_t \frac{I_f(V_f)R_s}{V_r}$$

Phase II - From $V_j \simeq 0$ to $V_j = -V_r$.

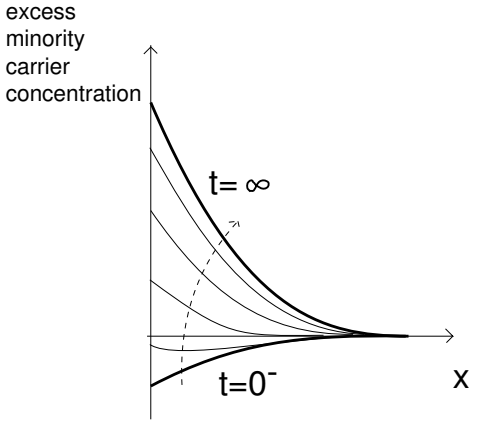
Charge depletion capacitance $\rightarrow R_s C_j$ time constant (as in Schottky diode).

⋆ Switch-on transient



$$I(0^-) = -I_s \qquad\qquad I(0^+) = \frac{V_f + V_r}{R_s}$$

Evolution of excess minority carrier concentration (long diode):



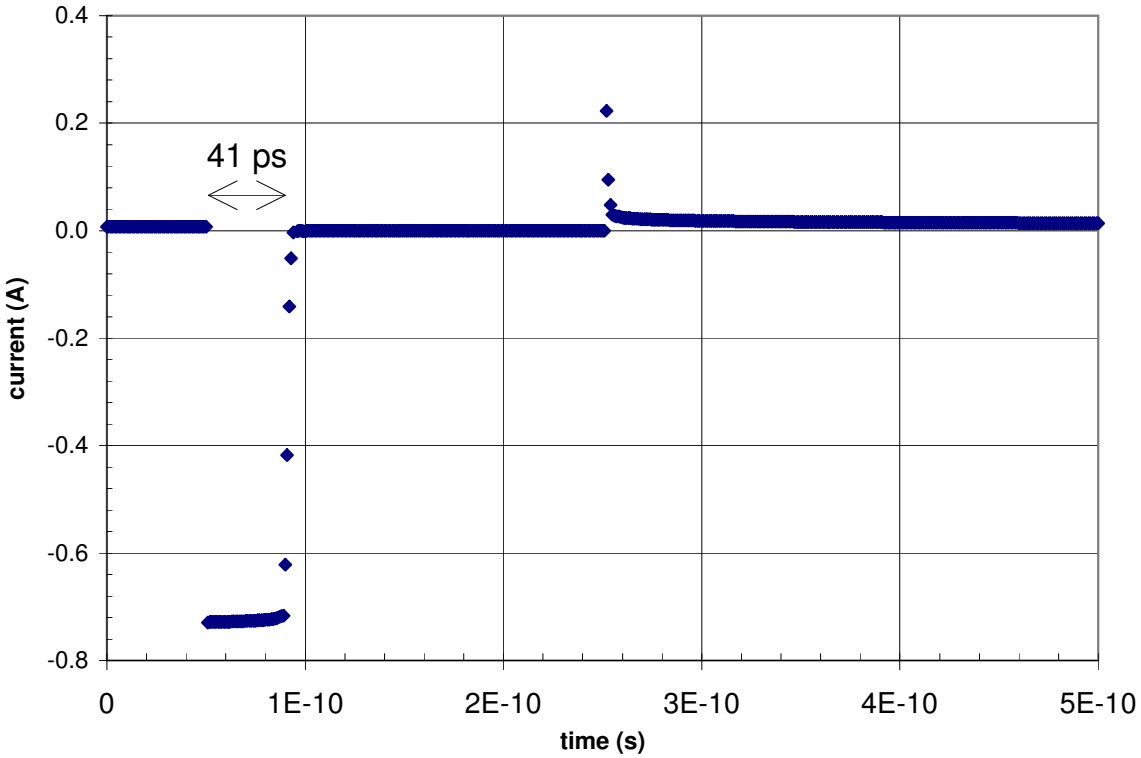
switch-on

- First, R_sC_j-type charge up of junction capacitance.
- Then, minority carrier charge injection → takes τ_t.

Example of SPICE simulations:

IS= $6e-17$, **N**= 1, **EG**= 1.12, **RS**= 8, **CJO**= $1.2e-13$, **VJ**= 0.6, **M**= 0.41, **XTI**= 3.814, and **TT**= $4e-9$

$V_f = +0.89\ V$, $V_r = -5\ V$



parameter	SPICE	hand calculation
t_{rr}	41 ps	46 ps
τ_{on}	2.6 ns	4 ns
I_{rr}	730 mA	736 mA
$I_f(pk)$	?	736 mA

Key conclusions

- *Diffusion capacitance* arises from minority carrier storage in QNR's and quasi-neutrality:

$$C_d = \frac{q}{kT}\Sigma_{n,p}(\text{dominant minority carrier time constant} \times \text{minority carrier current density})$$

- $C_d \propto J \propto \exp\frac{qV}{kT} \Rightarrow C_d$ dominates in forward bias, C_j dominates in reverse bias.
- Difficult to implemented integrated diodes in CMOS process: parasitic bipolar transistor.
- Dynamics of p-n diode dominated by minority carrier storage.
- *Reverse recovery time* is time required to eliminate minority carrier stored charge in switch-off transient.

Self study

- Diffusion capacitance in short diode.
- Equivalent circuit models for pn diode