6.334 Power Electronics
Spring 2007

Power Electronics Notes - D. Perreault

★★ DC/AC Inverters

★ Fourier Series Review

Break up a periodic signal as a sum of harmonically-related sin + cosine terms (or as a sum of complex exponentials)

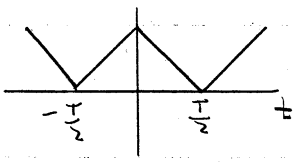
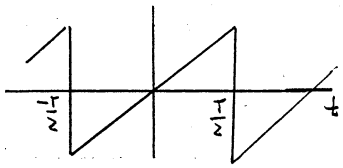
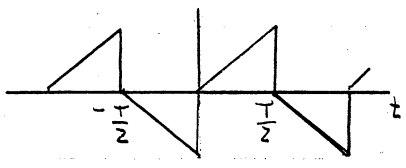
$$f(t) = \frac{b_0}{2} + \sum_{n=1}^{\infty} a_n \sin(n\omega_0 t) + b_n \cos(n\omega_0 t)$$

Coefficients can be calculated as:

$$a_n = \frac{2}{T} \int_{<T>} f(t) \sin(n\omega_0 t)\, dt$$

$$b_n = \frac{2}{T} \int_{<T>} f(t) \cos(n\omega_0 t)\, dt$$

Some waveforms have special characteristics

Even $X(t) = X(-t)$	Odd $X(t) = -X(-t)$	Half-wave symmetry $X(t) = -X(t - T/2)$
		
No Sin terms a_n's = 0	No Cos terms b_n's = 0	No Even harmonics a_{2k}'s, b_{2k}'s = 0 $k \in I$
Reason: calculating a_n's are integrals of even fn. times (odd) sines; result is odd ∴ integral = 0	calculating b_n's are integrals of odd fn times (even) cosines; result is odd ∴ integral = 0	Calculating a_{2k}, b_{2k}'s are integrals where 1st half of integral exactly cancels 2nd half ∴ integral = 0

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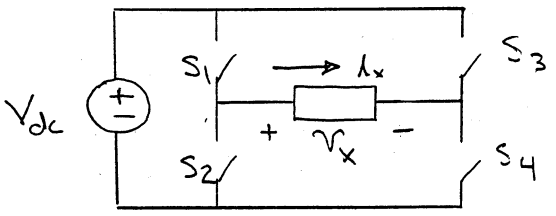
★ Inverter structure

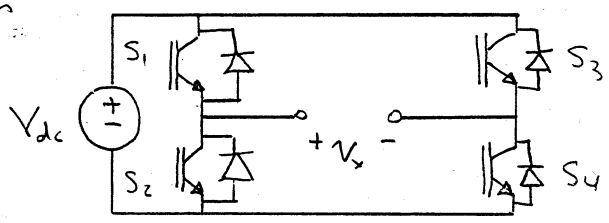
Suppose one wants to create an ac waveform from a dc source. This can be accomplished with a bridge of switches:



Switches on	v_x
S_1, S_4	$+V_{dc}$
S_2, S_3	$-V_{dc}$
S_1, S_3	0
S_2, S_4	0

If the load/filter is resistive or inductive in nature, the output current will lag the applied voltage. (i_x lags v_x) So switches block forward voltage but must carry bidirectional current

Ex/ Implementation



MOSFETs with their (internal) body diodes are often used

Suppose we want to synthesize a sinusoidal voltage.

★ Programmed PWM (KSV Section 8.2)

First: Simplest approximation of a sinusoid while switching each device on & off once per cycle

(allowed # of switchings can be limited by power dissipation)

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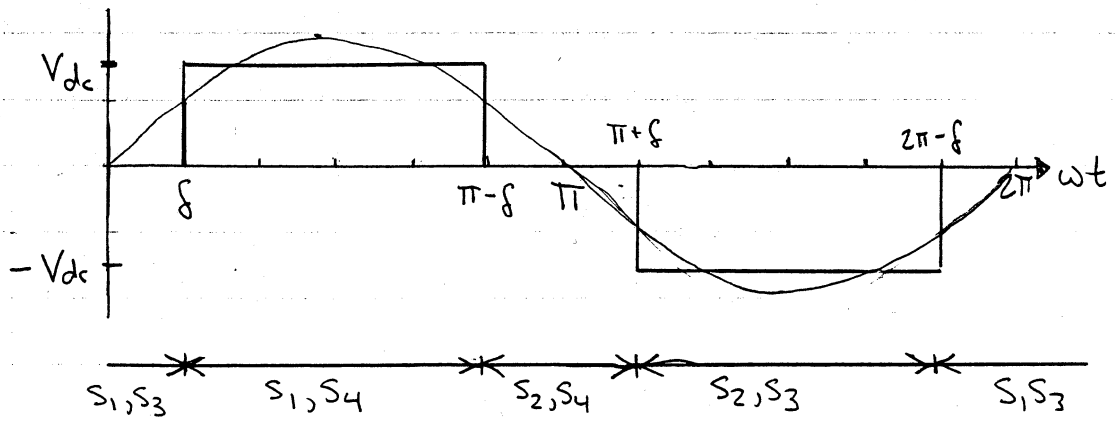


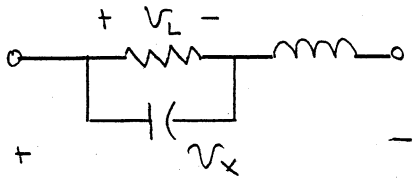
Odd waveform (in this case, synth sin) → no cos terms
Half-wave symmetric → no even harmonics (good!)

$$\therefore \quad V_x = \sum_{n\,odd} V_n \sin(n\omega_0 t)$$

ex/ @ $\delta = 0$ Square wave $V_x = \frac{4V_{dc}}{\pi} \sum_{n\,odd} \frac{1}{n} \sin(n\omega_0 t)$

fundamental + 3rd, 5th, 7th, etc.

If our load filters out harmonics:



V_L will be more pure than V_x, but hard to filter low harmonics, since they are so close to the desired fundamental

What can we control by varying δ?

1. Fundamental Magnitude
2. harmonic magnitudes

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1. Control of fundamental $\left\{ V_x = \sum V_n \sin(n\omega_0 t) \text{ , } n \text{ odd only} \right\}$

$$V_1 = \frac{2V_{dc}}{\pi} \int_{\delta}^{\pi-\delta} \sin(\varphi)\, d\varphi$$

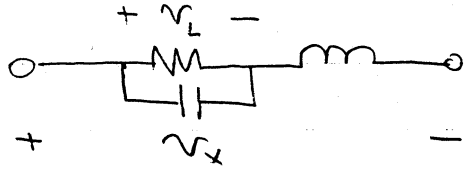
$$= \frac{2V_{dc}}{\pi} \left[\cos\delta - \cos(\pi - \delta) \right] = \frac{4V_{dc}}{\pi} \cos\delta$$

$\therefore$ by varying δ we can control the magnitude of the fundamental. This can be useful as a control handle.

2. We can also control harmonic magnitudes
(3rd harmonic is lowest nonzero harmonic)

$$V_3 = \frac{2V_{dc}}{\pi} \int_{\delta}^{\pi-\delta} \sin(3\varphi)\, d\varphi = \frac{4V_{dc}}{3\pi} \cos(3\delta)$$

If we choose $\delta = \pi/6$ (30°) $\Rightarrow V_3 \to 0$!!
So we can eliminate the 3rd harmonic by choosing δ properly (but cannot control the fundamental magnitude independently). Eliminating the 3rd harmonic leaves the 5th as lowest, + makes it easier to filter V_x to get the desired sinusoidal waveshape



← V_L has fundamental + attenuated harmonics. Higher harmonics attenuated more.

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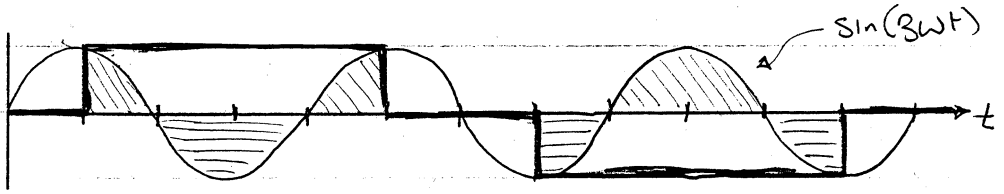
We can further reduce the harmonic content with Programmed PWM via Harmonic Elimination. That is the elimination of desired harmonics from the waveform by introducing appropriate notches.

The nth harmonic is determined as:

$$V_n = \frac{2}{T}\int_{<T>} f(t)\sin(n\omega_0 t)\,dt$$

So we consider the integral of the product of the n^{th} harmonic sinusoid + the PWM waveform:



Positive area of $f(t)\sin(3\omega t)$ cancels negative area $\rightarrow V_3 = 0$

→ we could introduce notches so that 5th harmonic is also cancelled, while not disturbing the 3rd harmonic cancellation. (see next page for one example.)

In general: Programmed PWM/Harmonic Elimination

→ One can eliminate one harmonic for each pulse in a half cycle. ⊓⊔⊓ 1 elim. ⊓⊔⊓⊔⊓ 2 elim., etc.

→ The more harmonics eliminated, the higher the switching freq.

→ Vx waveform harmonic content actually ↑, but low-frequency content ↓, making the waveform easy to filter.

→ Must switch at precisely controlled times (useful for μP control)

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Note: see classic papers for more on this area:

1. H. S. Patel and R. G. Hoft, "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I—Harmonic Elimination Techniques," *IEEE Trans. Industry Applications* IA-9 (3): 310–317 (May/June 1973).
2. H. S. Patel and R. G. Hoft, "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part II—Voltage Control Techniques," *IEEE Trans. Industry Applications* IA-10 (5): 666–673 (September/October 1974).

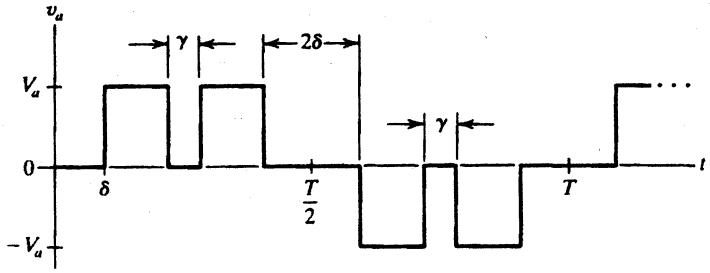

Figure 8.5 A tristate waveform containing notches of width γ.

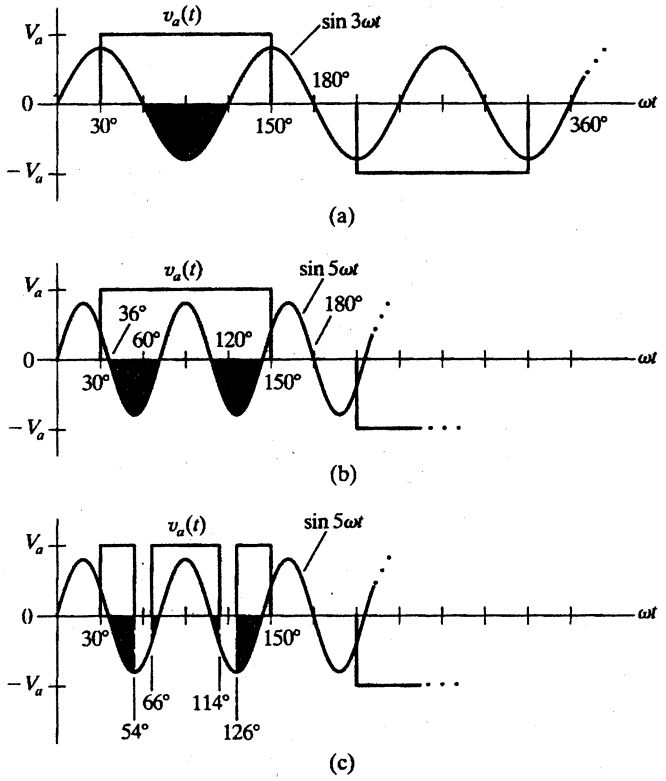

Figure 8.6 (a) Graphic representation of the integrand of *(8.14)*. The positive (lightly shaded) and negative (heavily shaded) areas are equal, canceling the third harmonic of the square wave. (b) The third-harmonic free waveform of (a) superimposed on a fifth-harmonic sine wave. (c) The square wave notched so that it is free from both third and fifth harmonics. A fifth-harmonic sine wave illustrates that the product of it and $v_a(t)$ has zero net area.

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★ Harmonic Cancellation

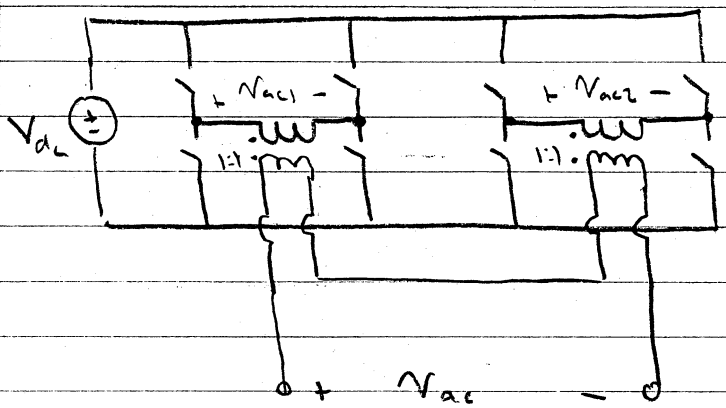
Add up time-shifted waveforms to cancel desired harmonic component(s)

If $x(t) = \sum A_n \sin(n\omega_0 t + \phi_n)$

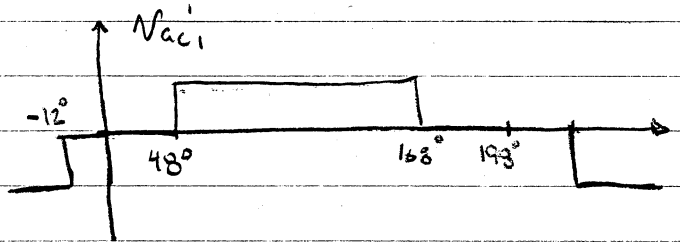
$\therefore x(t-t_1) = \sum A_n \sin(n\omega_0(t-t_1) + \phi_n)$

$= \sum A_n \sin(n\omega_0 t + \underbrace{\phi_n - n\omega_0 t_1}_{\phi_n'})$

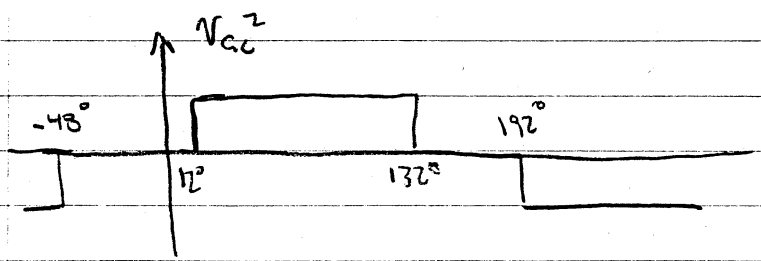
IF we time-shift to change the fundamental by an angle $\Delta\theta_1 = -\omega_0 t_1$, we shift the n^{th} harmonic by an angle $\Delta\phi_n = n\Delta\phi_1$



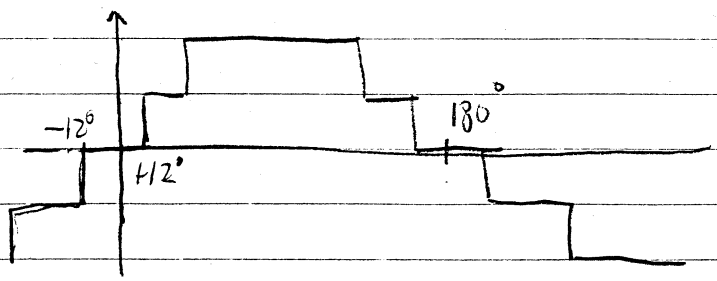
Sum 2 waveforms
→ shift fundamentals by 36° (±18°)
→ shifts 5th harmonics by 180° (±90°)



1st harm → shifted by +18°



Summed wave has no 5th harmonic



no third, 5th harmonic

by adding waveforms time shifted so that their 5th harmonics are 180° out of phase, the 5th harmonic is cancelled in the summed waveform!

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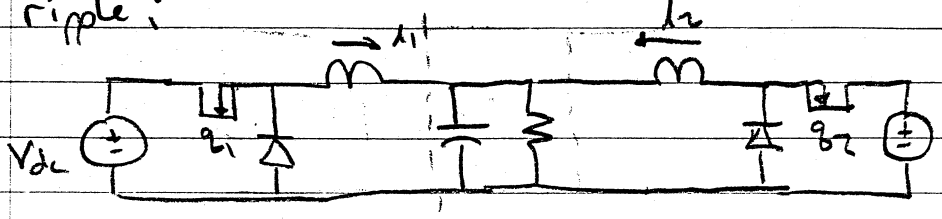
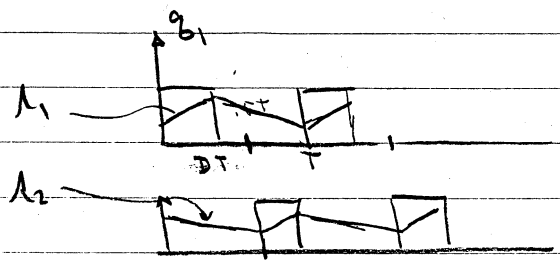
Note: This trick can be used to eliminate current ripple as well, and also in dc-output converters for ripple;

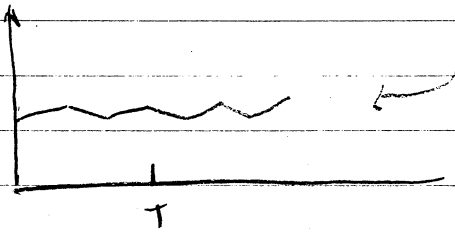


Interleaving

In this case, we want to cancel the fundamental.



Interleaving



fundamental ripple will beat $T/2$ $(2f_{sw})$

For N converters interleaved f_{ripple} ↑ by N

p-p magnitude ↓ by ≥ N

This is a classic trick. See Miwa, et. al. 1992 IEEE Applied Power Electronics Conf., pp 557-568 for a review. Also Chang, et. al IEEE Trans. Circ + Sys. I Vol. 42 No. 5 May 95, pp. 245-251 and Perreault, et. al., IEEE Trans. Circ. + Sys. I, Vol. 46, No. 10, Oct. 1999 pp. 1264-1274.

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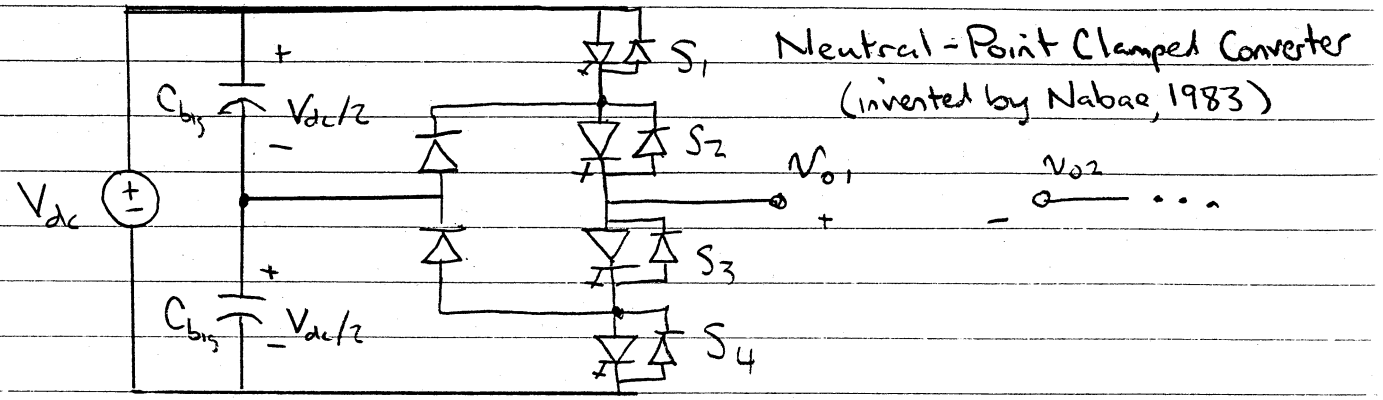
Other ways of achieving harmonic reduction also exist

★ **MULTILEVEL CONVERTERS**

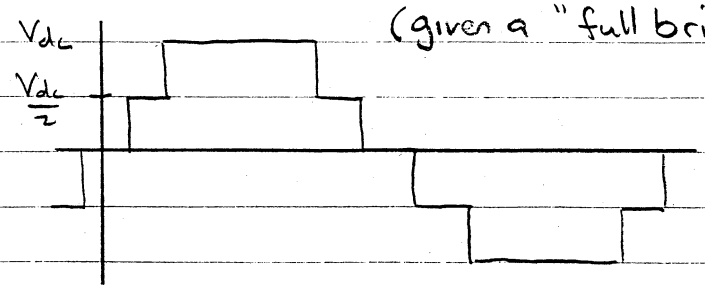


- Type of Multi-Level Inverter (3 level)
  - Very popular at high power levels
  - Even more level inverters can be made (≥ 7 level in use)

Switch State	v_{o1}	
$S_2 S_3$ ON	$V_{dc}/2$	Three levels (instead of 2) for one totem pole "leg"
S_1, S_2 ON	V_{dc}	
S_3, S_4 ON	0	

So we can generate 3 voltage levels 0, $V_{dc}/2$, V_{dc}

- Can implement waveforms like harmonic eliminated waveform of pg. 83 (or fancier multilevel PWM) (given a "full bridge" configuration)



- Each device only has to block $\frac{1}{2} V_{dc}$ so V_{dc} can be higher than individual device blocking voltage.
  - Higher-level versions expand this advantage

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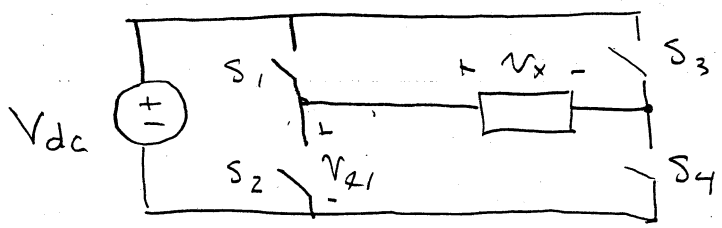
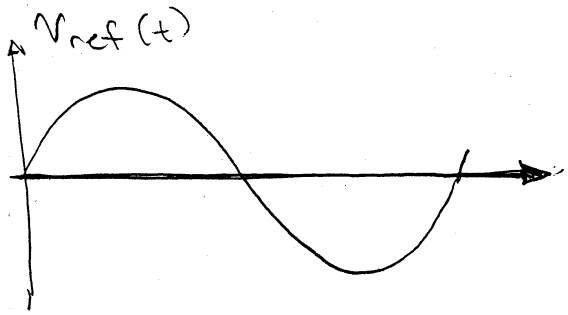
★ Sine-Triangle PWM

Suppose we can switch many times per cycle and would like the ability to synthesize an arbitrary waveform in real time.



If we want to make $\langle v_x \rangle$ follow a reference V_{ref} with $V_{ref} > 0$ part of the time and < 0 part of the time, we can modulate one way or the other

e.g.



If $V_{ref}(t) > 0$ {e.g. Pos ½ cycle}

Leave S_3 off, hold S_4 on

modulate S_1/S_2: $S_1: d(t) = \frac{V_{ref}(t)}{V_{dc}}$, $S_2: 1-d(t) = \frac{V_{ref}}{V_{dc}}$

If $V_{ref}(t) < 0$ {eg. negative half cycle}

Leave S_1 off, hold S_2 on

modulate S_3/S_4: $S_3: d(t) = \frac{|V_{ref}(t)|}{V_{dc}}$, $S_4: 1-d(t) = \frac{|V_{ref}|}{V_{dc}}$

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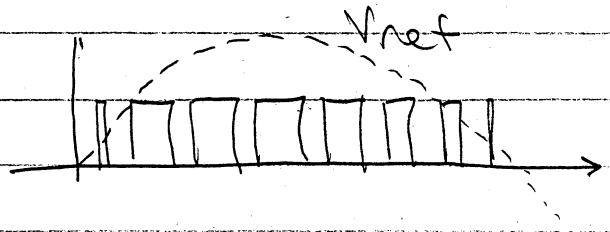
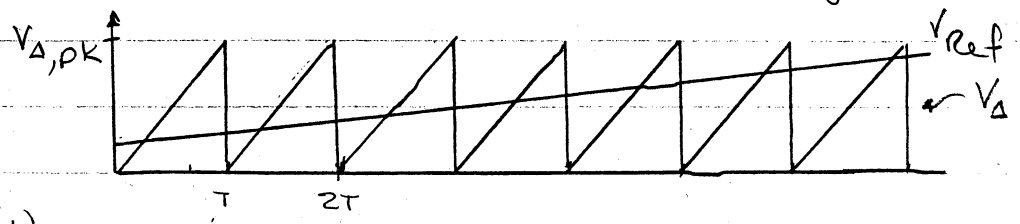
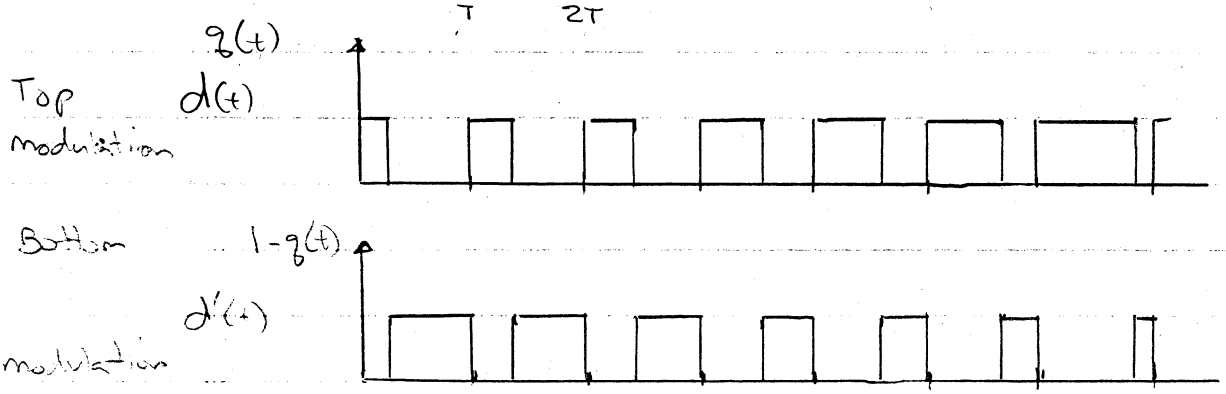
pos $\frac{1}{2}$ cycle



To implement modulating leg do "triangle intercept"



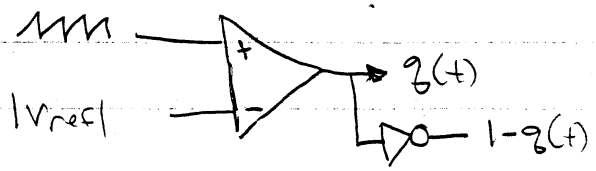
"leading" edge modulation



As long as $|V_{ref}| < |V_{\Delta,pk}|$ Then within a switching cycle $\langle q(t) \rangle = \left| \frac{V_{ref}}{V_{\Delta,pk}} \right| = d(t)$, so the average of v_x will be:

$$\langle v_x \rangle = \left| \frac{V_{ref}}{V_{\Delta,pk}} \right| \cdot V_{dc}$$

Implementation:



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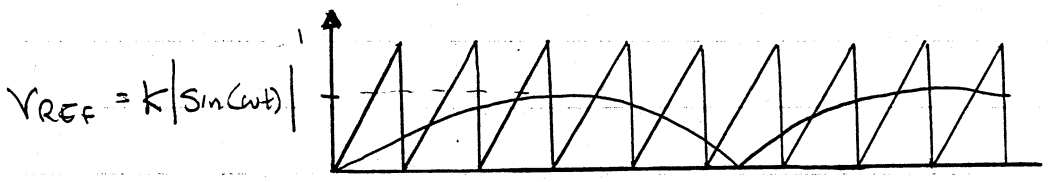
for sinusoidal $v_{ref}(t)$, $V_{a,pk} = 1$

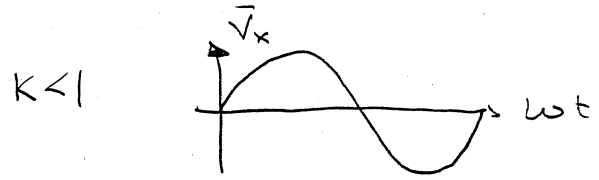


$$k \triangleq \frac{V_{ref,max}}{V_{dc}} = \text{depth of modulation}$$

local average over switching cycle

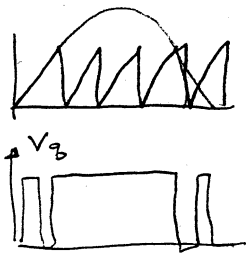
By varying k, we vary the magnitude of the fundamental voltage.

for $0 < k < 1$ $\quad \bar{v}_x = k V_{dc} \sin(\omega t)$



for $k > 1$ $\quad \bar{v}_x \neq k V_{dc} \sin(\omega t)$

since for some part of cycle $k|\sin(\omega t)| > 1$



This region is called overmodulation,

→ we do not get a sinusoidal $\bar{v}_x$, but fundamental of output voltage increases with k up to a limit

In extreme $k \gg 1$ → square wave output

$$V_1 = \frac{2}{2\pi}\int_0^{2\pi} V_x \sin\varphi \, d\varphi = \frac{4}{\pi} V_{dc}$$

as k reduces to 1 $\quad V_1 \to V_{dc}$

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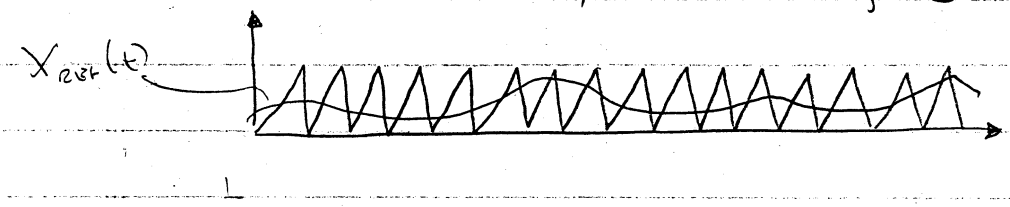
Note: There is no need for $V_{ref}(t)$ to be a sinusoid:
It can be an arbitrary waveform (e.g. Bach, Aerosmith, etc.)



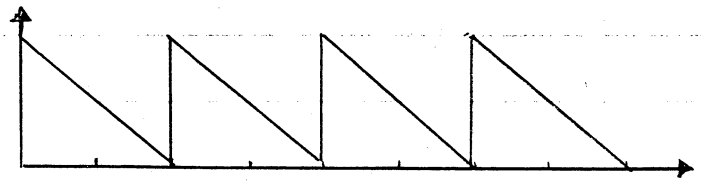
We will have good reproduction of the reference if

1. $|V_{ref}| < |V_{\Delta,max}|$
2. The frequency content of $V_{ref}(t)$ is much lower than f_{sw}.

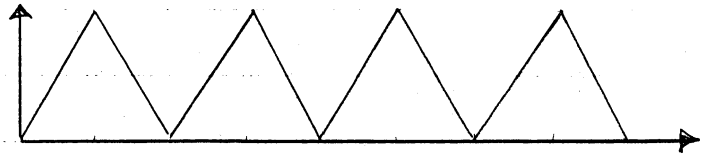
$\Rightarrow$ Switching audio amplifiers sometimes work this way

VARIATIONS:

Instead of using "Leading Edge" modulation, one can also use "trailing edge" or "double-sided": switching harmonic content varies a bit, but basic idea is same. (different ramp):



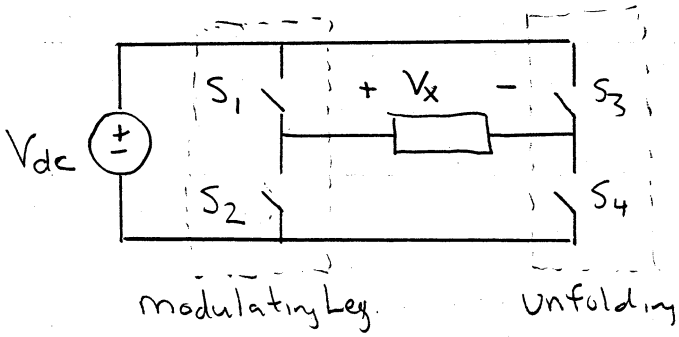
TRAILING EDGE



Double-sided

Alternative Methods of modulating the bridge are also possible:

Unfolding Method.



Another variant is to have assymetric use of the two bridge legs. One can always use one leg for doing the High-Frequency PWM modulation, and only use the second leg for "unfolding"

e.g. If $V_{ref} > 0$ → S_3 OFF, S_4 ON

→ S_1: PWM $d(t) = \frac{V_{ref}}{V_{dc}}$, S_2: $1-d(t) = \frac{V_{ref}}{V_{dc}}$

If $V_{ref} < 0$ → S_3 ON, S_4 OFF

→ S_1: PWM $1-d(t) = \frac{-V_{ref}}{V_{dc}}$, S_2: $d(t) = \frac{-V_{ref}}{V_{dc}}$.

This allows one to use fast-switching devices for S_1/S_2, while only needing Low-frequency switching devices (perhaps optimized for conduction loss) on the S_3/S_4 Leg. This technique is not as common in recent times due to good h.f. device availability

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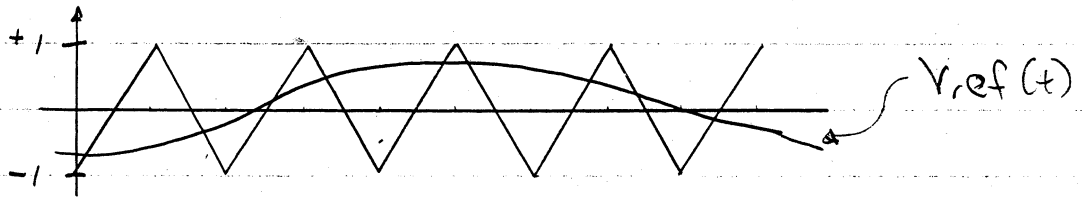
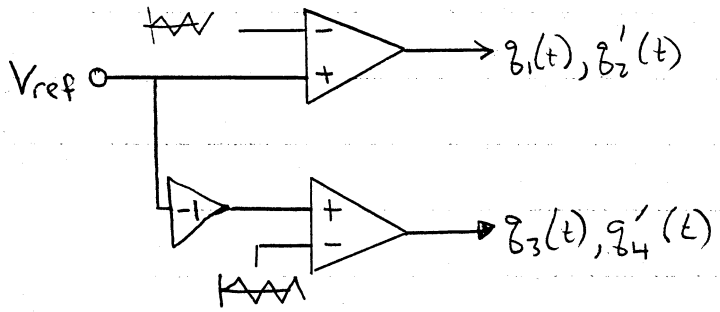
Simultaneous Modulation

One can also modulate both sides of the bridge at high frequency all the time. One typically uses a bipolar (positive and negative) ramp signal in this case:



To generate PWM signals appropriately



One incurs higher (switching) loss with this approach, but can get higher (switching) ripple frequency content in the output, so it is a tradeoff.

$V_{REF} > 0$	$V_{ref} > \Delta$, $-V_{REF} > \Delta$	S_1, S_3 on	0 state
	$V_{ref} > \Delta$, $-V_{ref} < \Delta$	S_1, S_4 on	$+V_{dc}$
	$V_{REF} < \Delta$, $-V_{REF} < \Delta$	S_2, S_4 on	0 state
$V_{REF} < 0$	Complement occurs		

Power Electronics Notes - D. Perreault

★ Inverter Current Control techniques

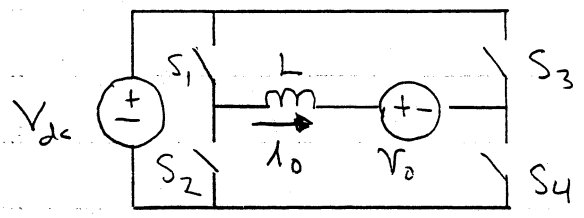
Instead of trying to synthesize a voltage directly, it is often better to make the inverter output <u>current</u> track a specified reference. (If desired we can then set the current reference to help us synthesize a desired voltage.)

This has a number of advantages

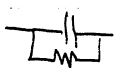
- → control converter currents, which directly relate to converter stresses + limitations (circuit protection)
- → allows "full state" feedback control including inductive filter or load. (improved system dynamics)
- → often we <u>want</u> to control current +/or can't control voltage (e.g. machine drive, line interfaced inverter)

{ For a review of inverter current control techniques, see DM Brod, DW Novotny "Current Control of VSI-PWM Converters" IEEE Trans. Ind. Appl. Vol. IA-21, No. 4, pp. 562-570, May/Jun 1985

Consider an inverter system with an inductive filter into a load:



v_o might be

1. The AC supply
2. RC load/filter 
3. Machine back EMF (with L as machine inductance)

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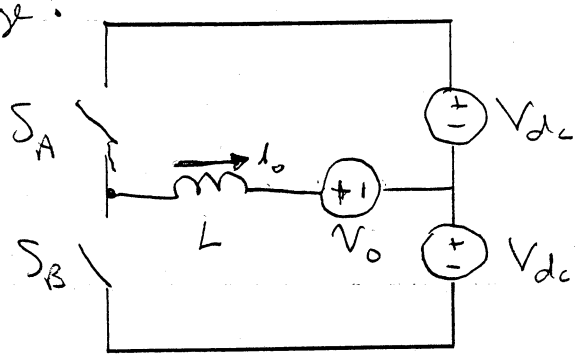
★ "Classic" Hysteresis Current Control

(cf AB Plunkett, 1979 IAS Annu. Mtg. pp 785-797)

Simple Version: S_1/S_4 on or S_2, S_3 on
→ equiv. to half bridge:

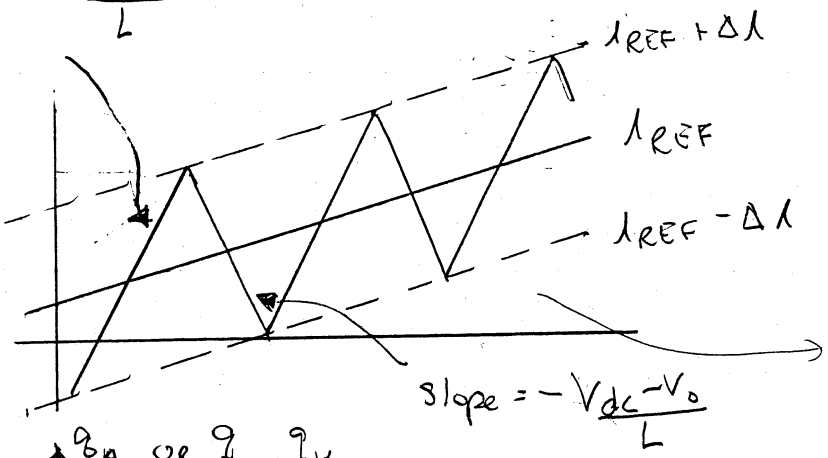


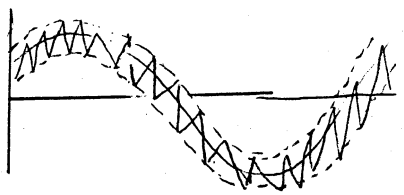
Compare i_o to i_{REF} (S_1/S_4 on) (S_2/S_3 off)

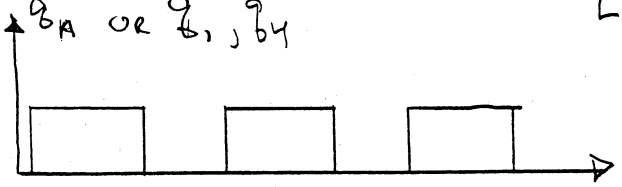
If $i_o < i_{REF} - \Delta i$ turn S_A on, S_B off

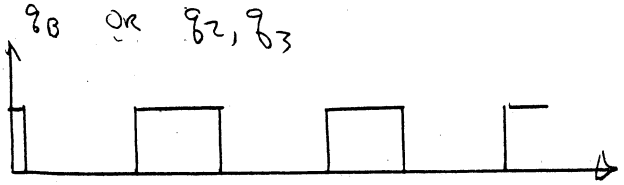
$i_o > i_{REF} + \Delta i$ turn S_B on, S_A off
(S_2/S_3 on) (S_1/S_4 off)

Slope $= \frac{V_{dc} - v_o}{L}$









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Switching based on keeping current within hysteresis bands.

f_{sw} varies dynamically:

$V = L\frac{\Delta i}{\Delta t}$

$\Delta t = \frac{L}{V}\Delta i$

$$T_{sw} = \Delta t_1 + \Delta t_2$$

$$= \frac{2L\Delta i}{(V_{dc} - V_o)} + \frac{2L\Delta i}{(V_{dc} + V_o)}$$

$$= \frac{4L\Delta i\, V_{dc}}{V_{dc}^2 - V_o^2} \Rightarrow \boxed{f_{sw} = \frac{V_{dc}^2 - V_o^2}{4L\Delta i\, V_{dc}}}$$

- f_{sw} drops drastically as V_o approaches V_{dc}. Must keep $V_{o,max}$ somewhat $< V_{dc}$ to keep $f_{sw} >> f_{line}$.
- f_{sw} varies significantly over a line cycle (e.g. if i_{ref}, V_o are sinusoidal)

- ripple current + total current are strictly controlled
- no zero-voltage state applied.

Many Variants!

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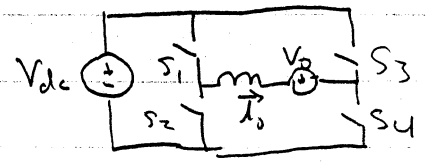


A Variant:

If $v_o > 0$ hold S_4 on

modulate S_1/S_2 to keep i_o in hysteresis band

→ If $i_o > i_{ref} + \Delta i \xrightarrow{\text{turn}} S_1$ off S_2 on

→ If $i_o < i_{ref} - \Delta i \xrightarrow{\text{turn}} S_1$ on S_2 off

If $v_o < 0$ hold S_2 on

modulate S_3/S_4 to keep i_o in hysteresis band

→ If $i_o > i_{ref} + \Delta i \xrightarrow{\text{turn}} S_3$ on, S_4 off

→ If $i_o < i_{ref} - \Delta i \xrightarrow{\text{turn}} S_3$ off, S_4 on

- Results in reduced switching frequency / losses for a given ripple current magnitude

- Can have trouble near zero crossing of v_o, since the driving voltage → 0 for one switching polarity (f_{sw} still varies greatly)
  → Additional tricks can be used in this case.

Another Variant: Make Δi a fn. of v_o. This helps keep f_{sw} constant over a line cycle, maintaining frequency separation between ripple + synthesized frequency.

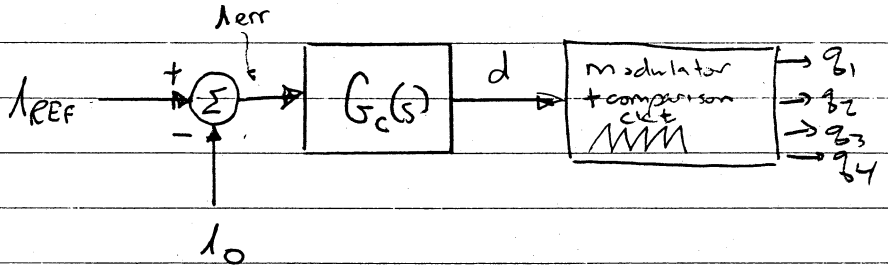
Another Variant: Constant off-time (not popular)

- Turn on until upper limit hit, then off for a specified time
- Has instantaneous i limit, Variable but limited switching freq.
- Similar troubles w/ zero crossings.

Power Electronics Notes - D. Perreault

★ Ramp Comparison Current Controller

- This technique is similar to the Sine-Triangle PWM Technique (p. 85) with the duty ratio signal for the PWM comparison derived from the error between actual output current and reference output current



(similar to "Average current-mode control" in dc/dc converters.

- any of the modulator schemes described for sine-triangle approach can be used

- switching frequency is fixed + produces well-defined ripple frequency content

- The compensator $G_c(s)$ must have a sufficiently low-pass nature that ripple in i_o does not feed through to the "d" signal. Otherwise, multiple comparator crossings can be problematic.

- Depending on the frequency content of i_{ref} (e.g. sinusoid at line frequency) The output current will have nonzero magnitude + phase error. This depends on the $G_c(s)$ that can be designed + the freq. content of the expected $i_{ref}(t)$

- instantaneous current limit is NOT achieved.

Power Electronics Notes

Predictive Current Controllers

- Discrete-time, microprocessor-based controllers
- At each time step T_k, measures V_o, I_o
- based on desired reference current at T_{k+1} $I_{k+1,ref}$ calculates average voltage V_x that must be applied to load. (discrete-time model)
  → Must have good model of the load ←

e.g. if $$V_x = R I_o + L \frac{dI_o}{dt} + V_o$$

$$\Rightarrow \quad V_{x,k} = \frac{R I_{REF,k+1} - I_{o,k} e^{-TR/L}}{1 - e^{-TR/L}} + V_{o,k}$$

Then calculates switching duty ratio in that cycle that will provide the correct V_x.

- fixed switching frequency; well-defined harmonics
- Complex hardware, computationally expensive, calculation time may limit bandwidth ⇒ expensive
- no instantaneous current limit
- one sample length of phase shift, but can get excellent performance if load model is good
- Variants exist for meeting various objectives (e.g. minimizing converter switching frequency

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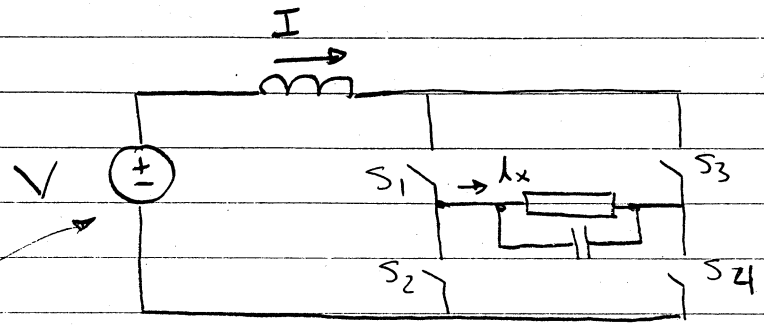
★ Other Inverter Structures:

Current-Source Inverter: (PWM Version)

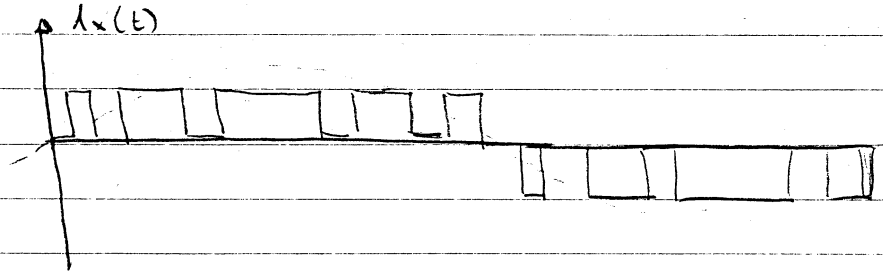


Dual of normal bridge converter

Usually from Φ-controlled or switching converter

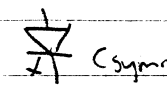
(mainly used in high-power 3Φ systems. Popular in 1980's, less so now).

- PWM Version can generate sinusoidal output voltage across filter cap.



- Inductor provides stiff current source
  → slow current rise in case of shoot through failure

- Positive conducting, Pos/Neg blocking devices needed

e.g.  (symmetric GTO) 

- The Current-Source Inverter (CSI) is the topological dual of the conventional Voltage-Source Inverter