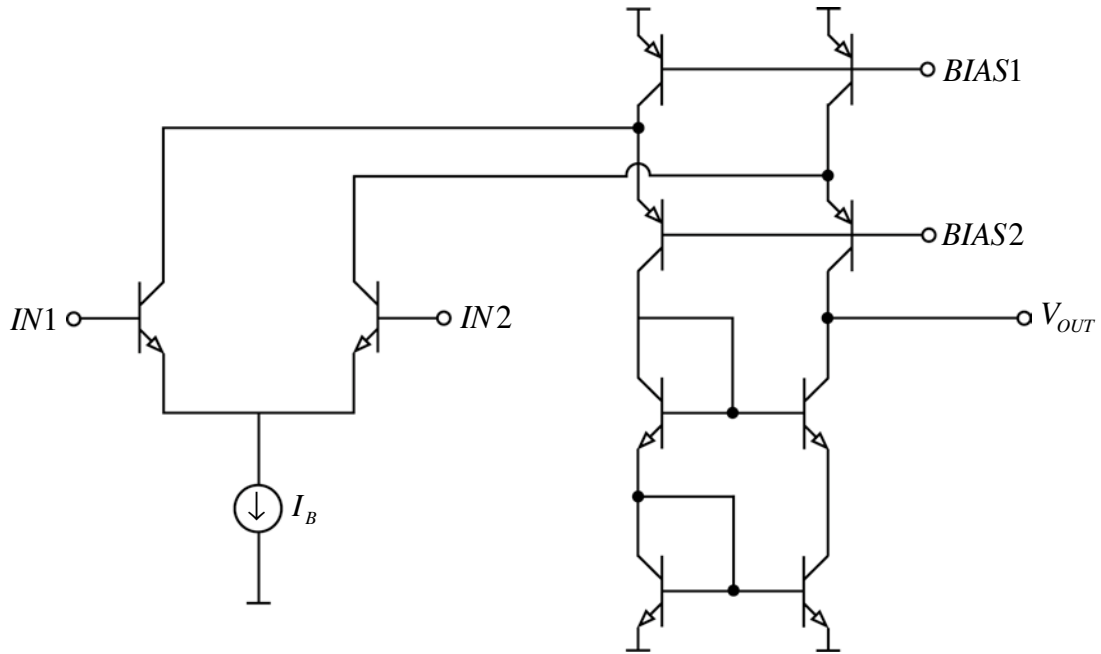


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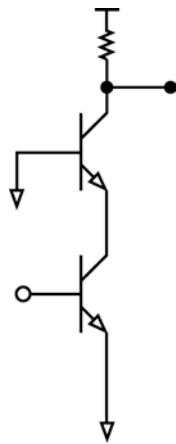
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CLASS EXERCISE: Consider the following single-stage operational amplifier.

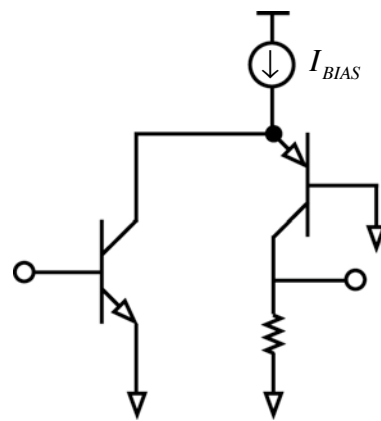


Determine which input is inverting, and which input is non-inverting.

This circuit uses a topology trick called a folded cascode:



Normal
Cascode



"Folded"
Cascode

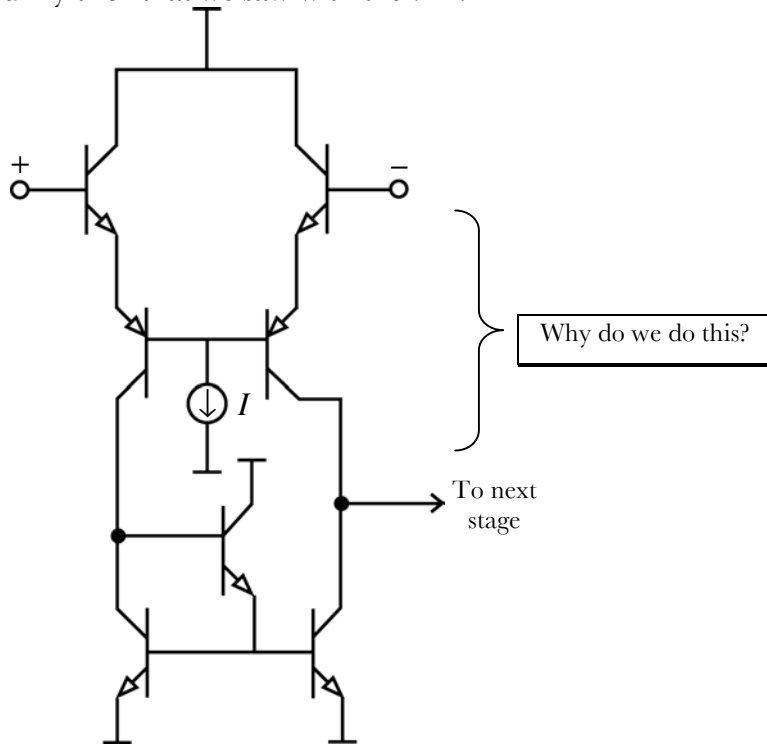
For the op-amps, it allows us to use a cascode current mirror without having to stack a large number of devices.

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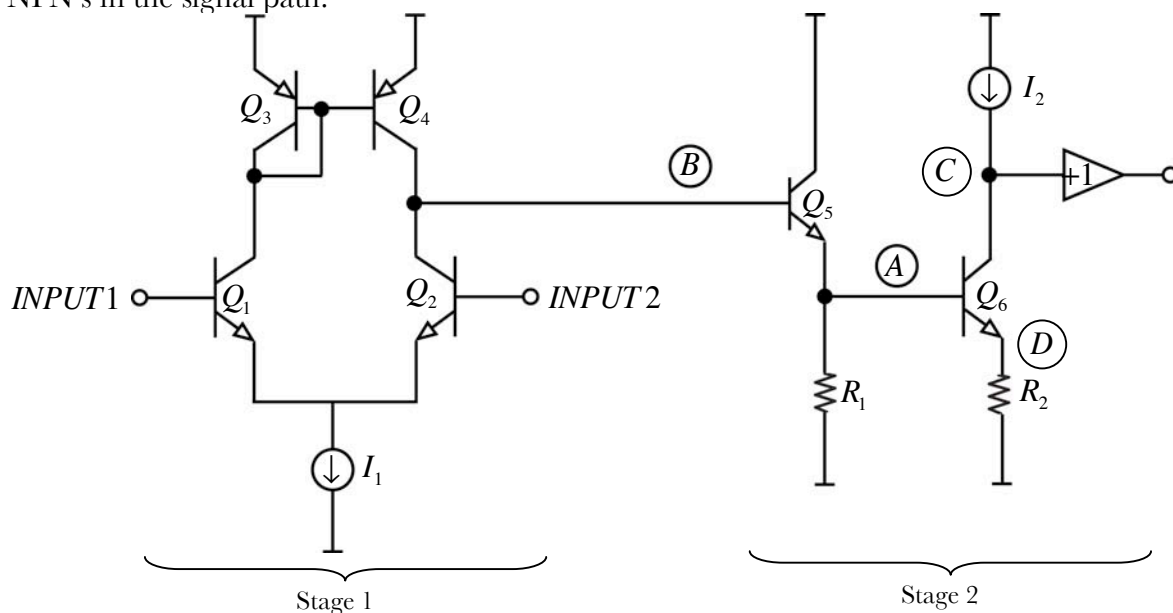
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Now let's continue our exploration of op-amp design tricks by looking at the LM101. If we draw out its input stage, we again see this funny trick that we saw with the 741:



There are a couple of problems that this input stage very clearly addresses. The first is the “level-shifting problem.” To see how this shows up, consider that in many processes, we'd prefer to use only NPN's in the signal path:



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The voltage at (A) is not going to be much higher than a V_{BE} above the negative supply rail. This is because we rely on stage 2 for a lot of gain, and a high voltage across R_2 implies a high degree of degeneration. To see this, consider that the gain of stage 2 is given approximately by

$$a_v = \left(\frac{g_m}{1 + g_m R_2} \right) r_{0,NPN} \parallel r_{0,PNP} = \left(\frac{g_m}{1 + g_m R_2} \right) \left[\frac{(1 + g_m R_2) V_{A,NPN}}{I_2} \parallel \frac{V_{A,PNP}}{I_2} \right]$$

Let $V_{A,NPN} = V_{A,PNP} = V_A$ (Devices have identical Early voltages.)


$$\text{Then, } \left[\frac{(1 + g_m R_2) V_{A,NPN}}{I_2} \parallel \frac{V_{A,PNP}}{I_2} \right] \Rightarrow \frac{1}{2 + g_m R_2} \left(\frac{V_A}{I_2} \right)$$

Now we can calculate the gain:

$$\begin{aligned} a_v &= \left(\frac{g_m}{1 + g_m R_2} \right) \left(\frac{1}{2 + g_m R_2} \right) \frac{V_A}{I_2} = \left(\frac{\frac{I_2}{V_T}}{1 + \frac{I_2}{V_T} R_2} \right) \left(\frac{1}{2 + \frac{I_2}{V_T} R_2} \right) \left(\frac{V_A}{I_2} \right) \\ &= \frac{V_A}{V_T} \left(\frac{1}{1 + \frac{I_2}{V_T} R_2} \right) \left(\frac{1}{2 + \frac{I_2}{V_T} R_2} \right) \end{aligned}$$

Now, $I_2 R_2 = V_D$, so

$$a_v = \frac{V_A}{V_T} \left(\frac{1}{2 + 3 \frac{V_D}{V_T} + \frac{V_D^2}{V_T^2}} \right) \approx \frac{V_A}{V_T} \frac{V_T^2}{V_D^2} = V_T V_A \frac{1}{V_D^2}$$


 Want V_D small!

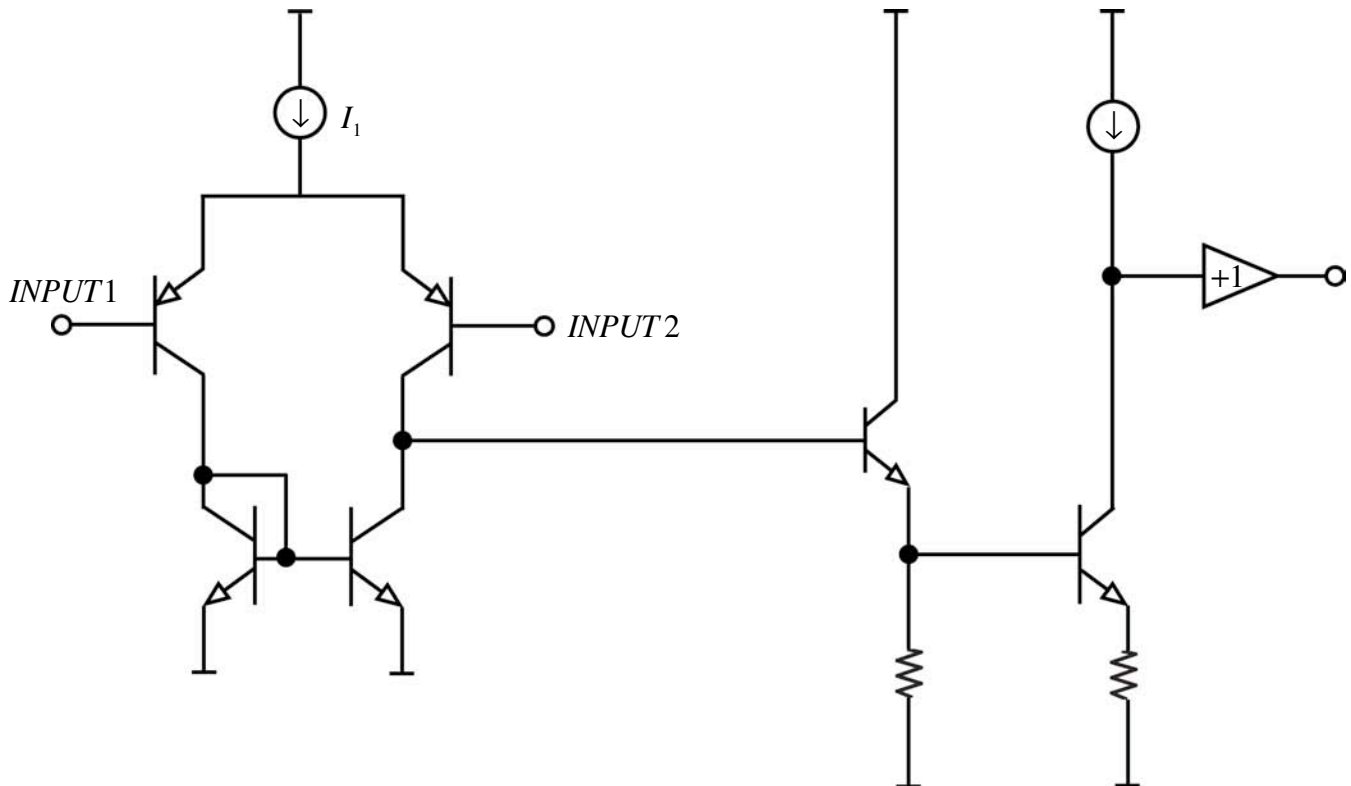
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The problem is that V_B is only a little more than $2V_{BE}$ above the negative supply rail. Suddenly, we're restricted to very low common-mode input levels!

This, in a nutshell, is the level-shifting problem. To see how PNP devices could help us, look at...



Now, of course, we have plenty of common-mode input range. This solution is fine if we have 2N3906s lying around (nice, high β_F s). But in the IC world, where β may be 5 for PNPs, and where PNPs are slow to boot, this solution gives a pretty poor input stage.

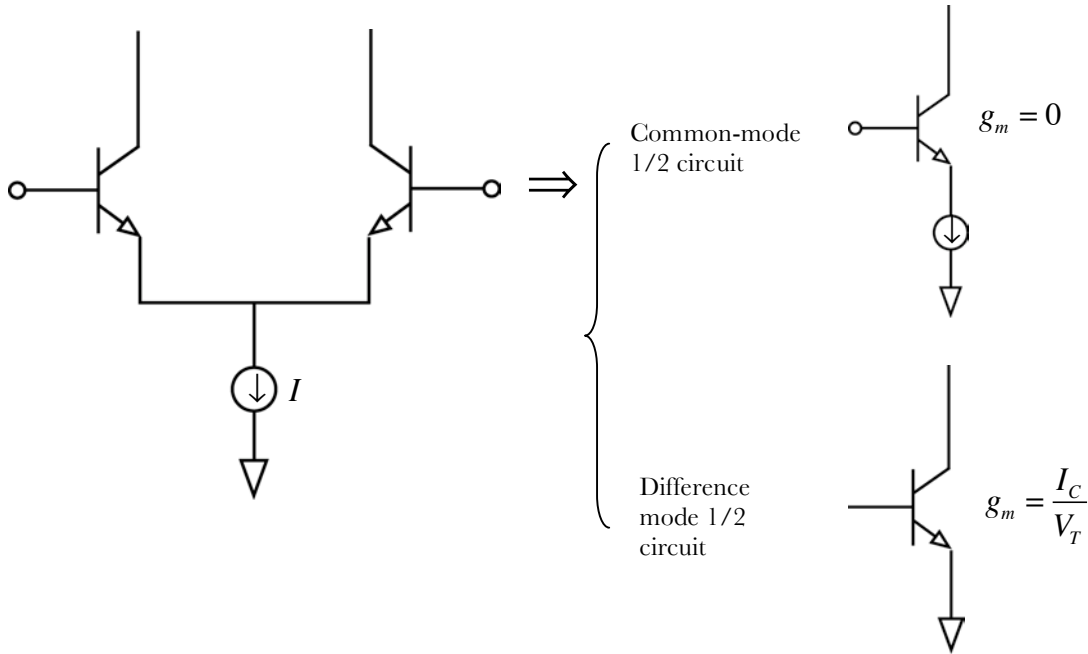
Looking back at the LM101 input stage, we can see that the emitter follower and common base input stage solves the level-shifting problem. Also, our input current now depends on β_F of the NPNs, and the common base configuration squeezes the most bandwidth we can out of the PNPs! Now let's just make sure we understand how this stage really functions...

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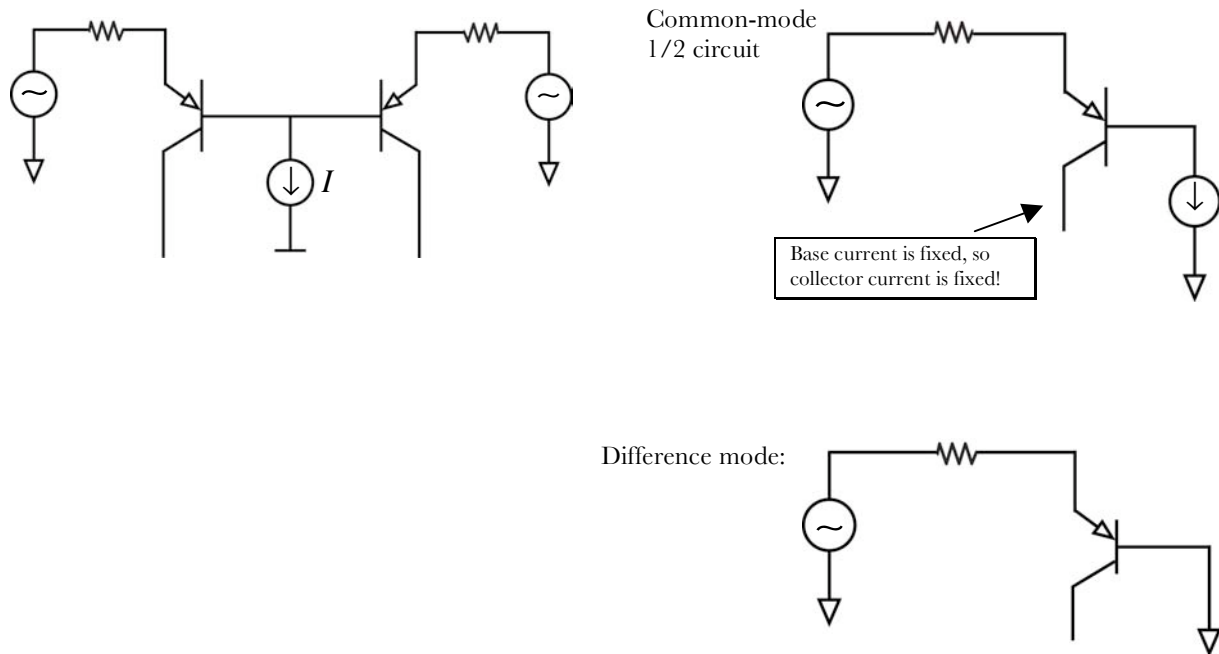
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An ordinary differential pair gives good differential g_m w/zero common-mode g_m :



Flipping things over for the common-base stage



Normal common-base stage

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