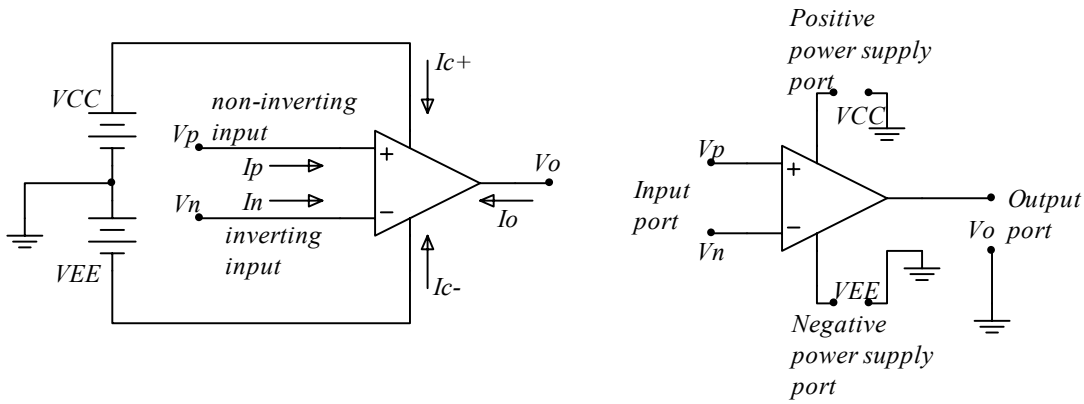
Operational Amplifiers

Introduction

The operational amplifier (op-amp) is a voltage controlled voltage source with very high gain. It is a five terminal four port active element. The symbol of the op-amp with the associated terminals and ports is shown on Figure 1(a) and (b).



(a) (b)

Figure 1. Symbol and associated notation of op-amp

The power supply voltages *VCC* and *VEE* power the operational amplifier and in general define the output voltage range of the amplifier. The terminals labeled with the "+" and the "-" signs are called non-inverting and inverting respectively. The input voltage *Vp* and *Vn* and the output voltage *Vo* are referenced to ground.

The five terminals of the op-amp form one (complicated) node and if the currents are defined as shown on Figure 1(a) the KCL requires that

$$In + Ip + Ic_{+} + Ic_{-} + Io = 0 \tag{1.1}$$

Therefore for current balance we must include all currents. This is what defines an active element. If we just consider the signal terminals then there is no relationship between their currents. In particular,

$$In + Ip + Io \neq 0 \tag{1.2}$$

The equivalent circuit model of an op-amp is shown on Figure 2. The voltage *Vi* is the differential input voltage $Vi = Vp - Vn$. *Ri* is the input resistance of the device and *Ro* is the output resistance. The gain parameter A is called the open loop gain. The open loop

configuration of an op-amp is defined as an op-amp circuit without any circuit loops that connect the output to any of the inputs. inputs.

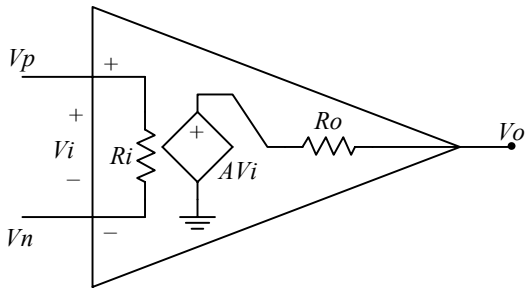


Figure 2. Equivalent circuit model of op-amp device

In the absence of any load at the output, the output voltage is

$$Vo = AVi = A(Vp - Vn) \tag{1.3}$$

Which indicates that the output voltage *Vo* is a function of the difference between the input voltages *Vp* and *Vn*. For this reason op-amps are **difference amplifiers**.

For most practical op-amps the open loop DC gain *A* is extremely high. For example, the popular 741 has a typical open loop gain *A* of 200000 V_o/V_i. Some op-amps have open loop gain values as high as 10^8 V_o/V_i.

The graph that relates the output voltage to the input voltage is called the voltage transfer curve and is fundamental in designing and understanding amplifier circuits. The voltage transfer curve of the op-amp is shown on Figure 3.

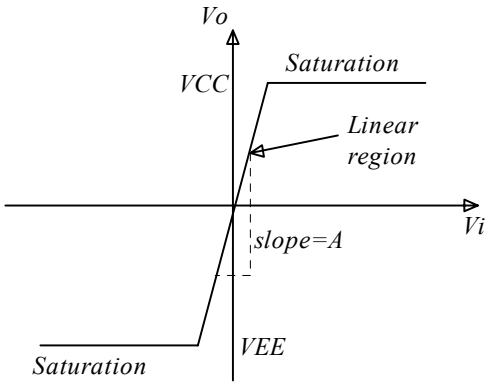


Figure 3. Op-amp voltage transfer characteristics.

Note the two distinct regions of operation: one around $Vi=0V$, the linear region where the output changes linearly with respect to input, and the other at which changes in Vi has little affect on Vo, the saturation region (non-linear behavior).

Circuits with operational amplifiers can be designed to operate in both of these regions. In the linear region the slope of the line relating Vo to Vi is very large, indeed it is equal to the open loop gain A. For a 741 op-amp powered with $VCC= +10V$ and $VEE= -10V$, Vo will saturate (reach the maximum output voltage range) at about $\pm 10\ V$. With an $A=200,000V/V$ saturation occurs with an input differential voltage of $10/200,000 = 50\mu V$, a very small voltage.

The ideal op-amp model

From a practical point of view, an ideal op-amp is a device which acts as an ideal voltage controlled voltage source. Referring to Figure 2, this implies that the device will have the following characteristics:

1. No current flows into the input terminals of the device. This is equivalent to having an infinite input resistance $Ri=\infty$. In practical terms this implies that the amplifier device will make no power demands on the input signal source.
2. Have a zero output resistance ($Ro=0$). This implies that the output voltage is independent of the load connected to the output.

In addition the ideal op-amp model will have infinite open loop gain ($A \to \infty$). The ideal op-amp model is shown schematically on Figure 4.

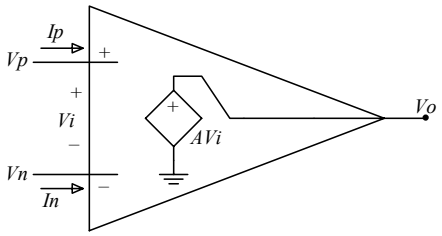


Figure 4. Ideal op-amp model.

In summary, the ideal op-amp conditions are:

$$\left.\begin{array}{ll} I_p = I_n = 0 & \text{No current into the input terminals} \\ R_i \to \infty & \text{Infinite input resistance} \\ R_0 = 0 & \text{Zero output resistance} \\ A \to \infty & \text{Infinite open loop gain} \end{array}\right\} \quad (1.4)$$

Even though real op-amps deviate from these ideal conditions, the ideal op-amp rules are very useful and are used extensively in circuit design and analysis. In the following sections we will see how to use these rules and the typical errors associated with these assumptions.

Note that when using the ideal op-amp rules we should remember that they are limits and so we must perform our analysis by considering them as limits. For example if we consider the equation

$$V_0 = AV_i \Rightarrow V_i = \frac{V_0}{A} \quad (1.5)$$

Which in turn implies that $V_i \to 0$ *as* $A \to \infty$. However, this does not mean that $V_0 \to 0$ but rather that as $A \to \infty$, $V_i \to 0$ in such a way that their product $AV_i = V_0 \neq 0$.

Negative Feedback and Fundamental Op-Amp Configurations.

By connecting the output terminal of the op-amp with the inverting terminal of the device we construct a configuration called the negative feedback configuration as shown on Figure 5. The presence of the biasing voltages of the op-amp, *VCC* and *VEE*, is assumed and will not be shown explicitly in the following circuits. The operational amplifier is assumed to be in the linear region (see Figure 3.)

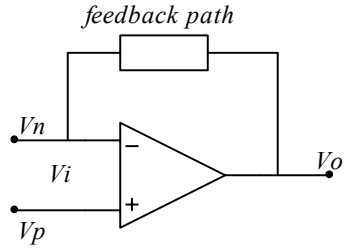


Figure 5. Basic negative feedback configuration.

The closed loop gain of this device is now given by the ratio:

$$G \equiv \frac{V_0}{V_i} \tag{1.6}$$

In negative feedback, a certain fraction of the output signal, voltage *Vo*, is fed back into the inverting terminal via the feedback path.

The block diagram configuration of the negative feedback amplifier is shown on Figure 6. This fundamental feedback circuit contains a basic amplifier with an open-loop gain *A* and a feedback circuit described by the parameter β.

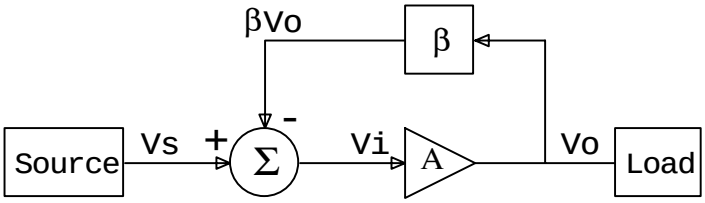


Figure 6. Block diagram of an ideal negative feedback amplifier

The feedback circuit provides a fraction of the output signal, βVo, which is **subtracted** from the input source signal, Vs. The resulting signal, Vi, which is also called the error signal, is the input to the amplifier which in turn produces the output signal Vo = AVi. It is the subtraction of the feedback signal from the source signal that results in the negative feedback.

The gain Vo/Vs of the inverting amplifier is given by

$$G \equiv \frac{Vo}{Vs} = \frac{A}{1+\beta \mathrm{A}} \tag{1.7}$$

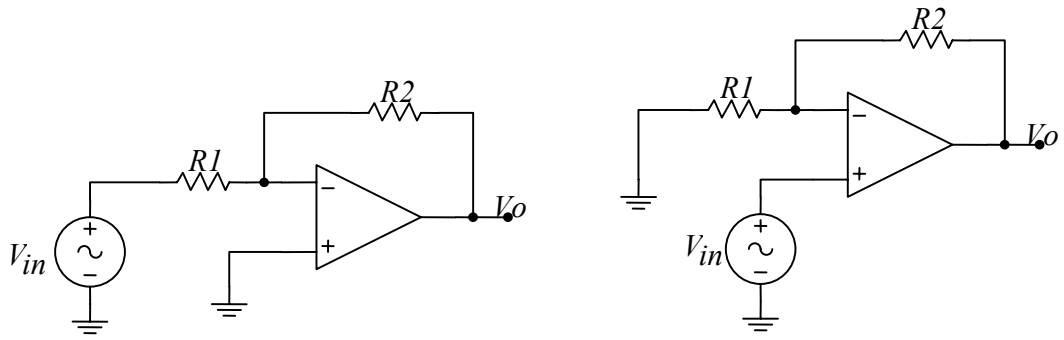
The feedback gain, or closed-loop gain, depends on the open-loop gain, A, of the basic amplifier and the feedback parameter β. The feedback parameter β depends only on the characteristics of the feedback network. For practical operational amplifiers the open-loop gain A is very large. Therefore, in the limit where $A \to \infty$, Equation (1.7) gives

$$G \cong \frac{1}{\beta} \tag{1.8}$$

and so the gain becomes independent of A and it is only a function of the parameter β. The value and "quality" of β depend on the design of the feedback network as well as on the "quality" of the elements used. Therefore, the designer of the feedback amplifier has control over the operational characteristics of the circuit.

Building Negative Feedback Amplifiers.

With two resistors we can construct the fundamental feedback network of a negative feedback amplifier. Depending on the terminal at which the signal is applied, the fundamental negative feedback configuration can be in the **inverting amplifier arrangement**, where the input signal, *Vin*, is applied to the inverting terminal, Figure 7(a), or in the **non-inverting amplifier arrangement**, where the input signal, *Vin*, is applied to the non-inverting terminal, Figure 7(b).



(a) Inverting amplifier (b) Non-inverting amplifier

Figure 7. Basic feedback amplifier configurations: (a) inverting, (b) non-inverting

We will perform the analysis by considering both the effect of finite open loop gain (A is finite) and the ideal op-amp model for which $A \to \infty$.

Inverting Amplifier

The basic inverting amplifier configuration is shown on Figure 8. The input signal, V_{in}, is applied to the inverting terminal and the balance of the circuit consists of resistors *R1* and *R2*.

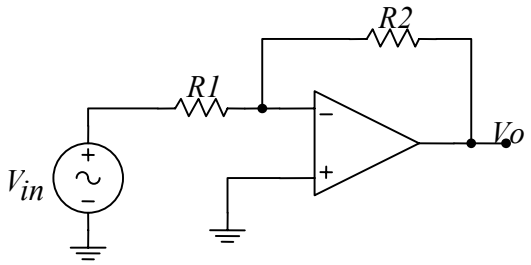


Figure 8. Inverting amplifier circuit

Let's analyze this circuit, i.e determine the output voltage *Vo* as a function of the input voltage *Vin* and the circuit parameters, by assuming infinite input resistance at the inverting and non-inverting terminals, zero output resistance and finite open loop gain *A*. The equivalent circuit of this model is shown on Figure 9.

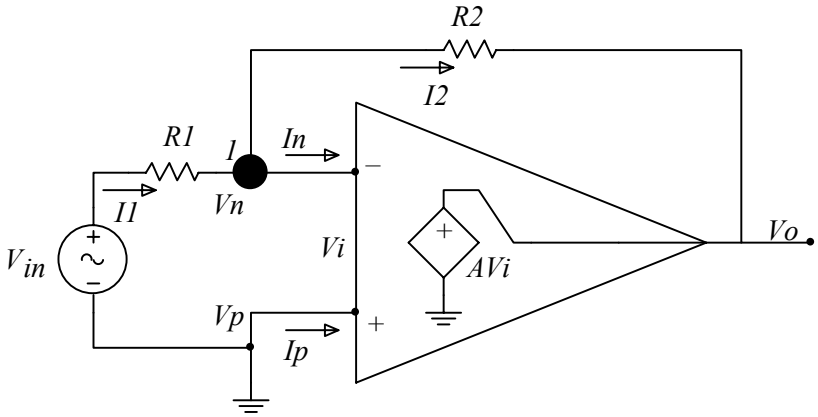
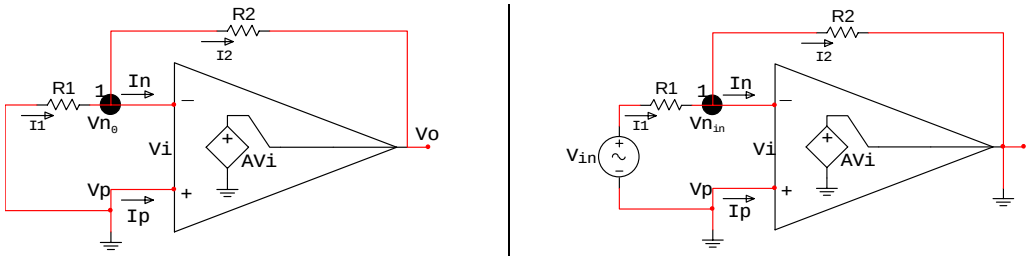


Figure 9. Inverting amplifier circuit model

Since our circuit is linear, the voltage at node 1 can be found by considering the principle of superposition.

Vn is the sum of voltages Vn_o and Vn_{in} as shown on the circuits of Figure 10.
Vn_o is the contribution of *Vo* acting alone and Vn_{in} is the contribution of *Vin* acting alone.



$$V_{n_o} = V_o \frac{R_1}{R_1 + R_2} \qquad V_{n_{in}} = V_{in} \frac{R_2}{R_1 + R_2}$$

Figure 10. Inverting amplifier equivalent circuits considering the property of linearity.

Vn is thus given by

$$V_n = V_{n_o} + V_{n_{in}} = V_o \frac{R_1}{R_1 + R_2} + V_{in} \frac{R_2}{R_1 + R_2} \tag{1.9}$$

The term $V_o \frac{R_1}{R_1 + R_2}$ corresponds to the output voltage that is fed back into the inverting input by the feedback resistor network.

We also know that $Vo = A(Vp - Vn)$ and since $Vp = 0$, $V_n = -\frac{V_o}{A}$. Equation (1.9) becomes

$$-\frac{V_o}{A} = V_o \frac{R_1}{R_1 + R_2} + V_{in} \frac{R_2}{R_1 + R_2} \tag{1.10}$$

By rearranging Equation (1.10) we obtain the voltage gain of the inverting amplifier

$$\begin{aligned} G \equiv \frac{V_0}{V_{in}} &= -\frac{A}{1 + \frac{R1}{R2}(1 + A)} \\ &= -\frac{R2}{R1} \frac{1}{1 + \frac{1}{A}\left(1 + \frac{R2}{R1}\right)} \end{aligned} \tag{1.11}$$

Recall that for an ideal operational amplifier the open loop gain A is infinite. By taking the limit of Equation (1.11) as $A \to \infty$, the "ideal" gain of the inverting amplifier becomes

$$G_{ideal} = \frac{V_0}{V_{in}} = -\frac{R2}{R1} \tag{1.12}$$

By comparing Equation (1.12) to Equation (1.8) we see that the feedback parameter for this amplifier circuit is $\beta = \frac{R1}{R2}$.

Note that the ideal gain depends only on the ratio of resistors *R1* and *R2*. This is a great result. We are now able to design an amplifier with any desirable gain by simply selecting the appropriate ratio of *R1* and *R2*. However, this design flexibility requires a very large value of *A*, the open loop gain of the op-amp. In practice this is not a very difficult requirement to achieve. Op-amp devices have been designed and manufactured with very low cost and are characterized by very high values of *A*.

The negative sign for the gain indicates that the polarity of *Vo* is opposite to the polarity of *Vin*. For example if the input signal *Vin* is a sinusoid of phase 0 degrees, the output signal will also be a sinusoid with a phase shift of 180 degrees. Figure 11 shows the voltages *Vin* and *Vo* for an inverting amplifier with *R2/R1=2*.

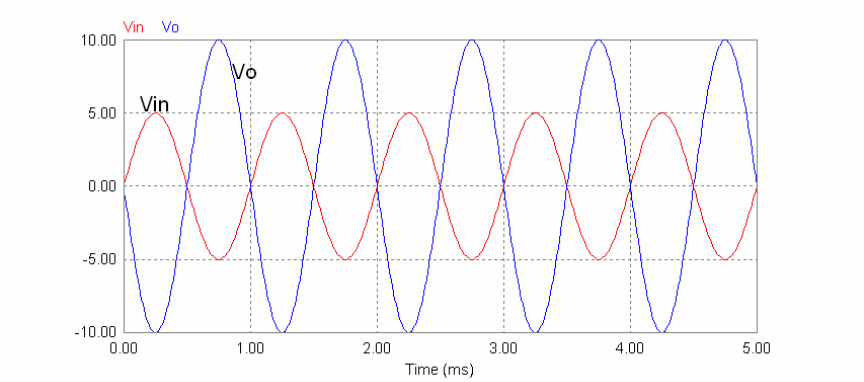


Figure 11. Input and output signals of an inverting amplifier with gain of 2.

It is instructive at this point to investigate the difference between the ideal model represented by Equation (1.12) and the finite open loop gain model represented by Equation (1.11). Let's consider an inverting amplifier design with *R1=10kΩ* and *R2=100kΩ*. In this case, the ideal voltage gain is -10 as given by Equation (1.12). By assuming that *A* ranges in values from 1,000 V/V to 10,000,000V/V, Table I shows the results from Equation (1.11) and the resulting deviation in % from the ideal case.

Table I. The effect of finite A on op-amp gain

A	G	Deviation %
1000	-9.9810	1.088
10000	-9.9890	0.109
100000	-9.9989	0.011
200000	-9.9998	0.0055
1000000	-9.9999	0.0011
10000000	-9.99999	0.00011

The widely used 741 op-amp has a typical open loop gain of 200,000 V/V. With the 741 used in an inverting amplifier circuit, the error introduced in the analysis by considering the ideal gain is less than 0.0055% (55 ppm), a very good value for many applications.

Inverting Amplifier. Ideal op-amp circuit analysis

The ideal op-amp rules are:

1. The differential input voltage is zero. $Vi = 0 \rightarrow Vn = Vp$
2. No current flowing into the input terminals. This is equivalent to infinite input resistance for the op-amp Ri = ∞ $In = Ip = 0$
3. Infinite open loop gain. $A \rightarrow \infty$
4. Output resistance is zero $Ro = 0$

By using these rules we can analyze the inverting amplifier op-amp circuit. From Figure 12 we see that *Vp* is at ground potential (*Vp=0V*). According to the second rule the voltage *Vn* must also be at zero Volts. This does not mean that the inverting terminal is grounded. It simply implies that the inverting terminal is at ground potential (zero volts) but it does not provide a current path to ground. This terminal is said to be at "virtual ground".

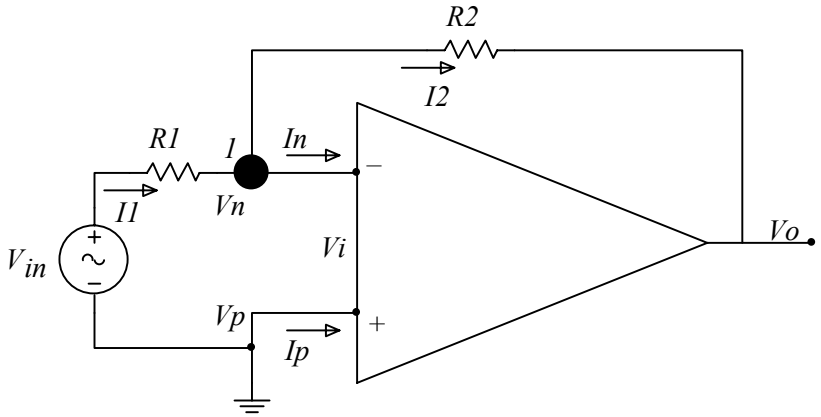


Figure 12. Ideal op-amp inverting amplifier circuit.

Since *In=Ip=0* (rule 2), KCL at node 1 tells us that current *I1* must be equal to current *I2*.

$$I1 = \frac{V_{in} - V1}{R1} = \frac{V_{in}}{R1} = I2 \qquad (1.13)$$

The current *I2*, flowing through *R2*, is related to the voltage drop across *R2*

$$I2 = \frac{Vn - Vo}{R2} \Rightarrow Vo = -I2\,R2 = -Vin\frac{R2}{R1} \tag{1.14}$$

And so the gain of the ideal inverting amplifier is

$$G_{ideal} \equiv \frac{V_0}{V_{in}} = -\frac{R2}{R1} \tag{1.15}$$

Note that the gain given by Equation (1.15) is the same as that obtained in the general case as given by Equation (1.11) as $A \to \infty$.

In order to obtain additional intuition on the operation of this circuit let's consider the two cases for *Vin*.

1. For *Vin >0* the current *I1* will be flowing as indicated on Figure 12. Since *In = 0*, *I2* must also flow as indicated. In order for this to happen, the voltage *Vo* must be at a lower potential than the voltage *Vn*. But since *Vn=0*, this can happen only if *Vo < 0*.

2. For *Vin <0* the direction of the currents will be reversed and the argument follows in a similar way, resulting in *Vo > 0*.

Non-Inverting Amplifier

Figure 13 shows the basic non-inverting amplifier configuration. The negative feedback is maintained and the input signal is now applied to the non-inverting terminal.

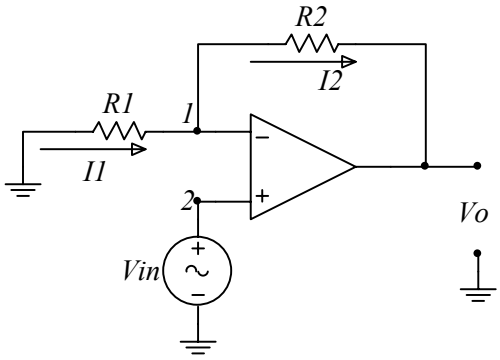


Figure 13. Non-inverting amplifier

The equivalent circuit of the Non-Inverting amplifier with a finite open-loop gain is shown on Figure 14. Here we have assumed an infinite input resistance and a zero output resistance for the op-amp.

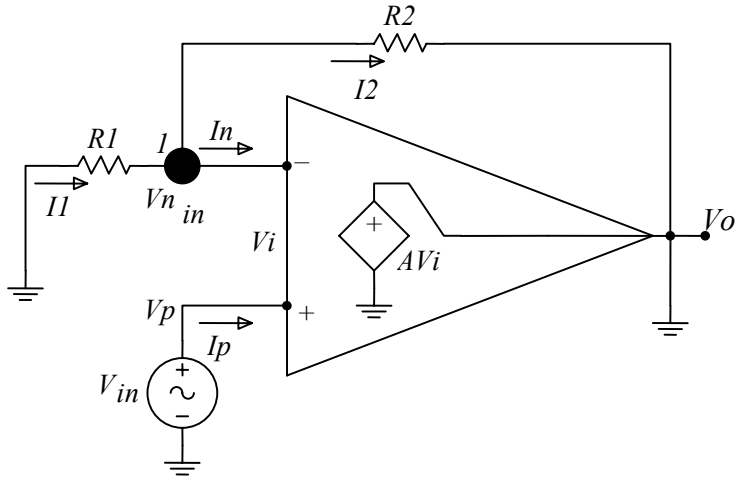


Figure 14. Equivalent circuit of Non-inverting amplifier with finite open loop gain.

Since $In = Ip=0$, we have $I1=I2$ and therefore:

$$\frac{-Vn}{R1}=\frac{Vn-Vo}{R2}\Rightarrow\frac{Vo}{R2}=Vn\left(\frac{1}{R1}+\frac{1}{R2}\right) \tag{1.16}$$

Since the voltage $Vi = Vp\text{-}Vn = Vin\text{-}Vn$, the output voltage is given by:

$$Vo = A(Vin - Vn) \tag{1.17}$$

Combining Equations (1.16) and (1.17), the resulting expression for the closed loop gain, $G \equiv \frac{Vo}{Vin}$, becomes:

$$G \equiv \frac{Vo}{Vin} = \frac{1 + R2/R1}{1 + (1 + R2/R1)/A} \tag{1.18}$$

The gain is positive and unlike the inverting amplifier, the output voltage *Vo* is in phase with the input *Vin* and the gain is always greater than 1.

From Equation (1.18)we see that as $A \to \infty$, the closed loop gain is

$$\underset{A\to\infty}{G} = 1 + \frac{R2}{R1} \tag{1.19}$$

The open-loop gain, *A*, of an op-amp is a parameter with considerable variability. It depends on the characteristics of the various components inside the operational amplifier (transistors, resistors, capacitors, diodes) and so it may be a function of environmental conditions (temperature, humidity) and manufacturing processes. As *A* changes by a certain fraction, $\frac{dA}{A}$, the closed loop gain, *G*, will also change by an amount $\frac{dG}{G}$. By taking the derivative $\frac{dG}{dA}$ of Equation (1.18) and simplifying we obtain:

$$\frac{dG}{G} = \frac{dA}{A}\left[\frac{1 + \frac{R2}{R1}}{1 + \frac{1 + \frac{R2}{R1}}{A}}\right] = \frac{dA}{A}\left(\frac{G}{A}\right) \tag{1.20}$$

From Equation (1.20) we see that the change in *G* due to a change in *A* is modulated by the factor $\frac{G}{A}$.

As an example let's consider the 741 op-amp with a nominal open loop gain of 200 *V/mV*, which is arranged in a non-inverting amplifier configuration with a closed loop gain of 10. If the open loop gain *A* changes by 20%, the change in the closed loop gain as given by Equation (14) is

$$\frac{dG}{G} = 20\left(\frac{10}{2.0\times10^5}\right)\% = 0.001\% \tag{1.21}$$

The advantage of having an op-amp with a large value of A is apparent. Of course by "large" value we mean that the open-loop gain is much larger than the closed loop gain $(A >> G)$.

We have been able, by using a component that is characterized by large uncertainty in its performance, to construct a devise with very high performance. This however can happen only if the open-loop gain A is very large, which can be easily achieved with standard integrated circuit technology.

Non-inverting amplifier: Ideal model

Referring to Figure 13, the ideal model implies the voltages at nodes 1 and 2 are equal: $Vn = Vin$. Also, since no current flows into the terminals of the op-amp, KCL at node 1 gives,

$$\left.\begin{aligned} I1 &= I2 \\ I1 &= -\frac{Vin}{R1} \\ I2 &= \frac{Vin - Vo}{R2} \end{aligned}\right\} \Rightarrow -\frac{Vin}{R1} = \frac{Vin - Vo}{R2} \tag{1.22}$$

Solving for the gain (Vo/Vin) we have,

$$G \equiv \frac{Vo}{Vin} = 1 + \frac{R2}{R1}\bigg|_{ideal} \tag{1.23}$$

Note that Equation (1.23) is the same as Equation (1.19) which was obtained in the limit as $A \to \infty$.

Voltage Follower. Buffer.

By letting $R1 \to \infty$ and $R2 = 0$, Equation (1.23) gives $G = \frac{Vo}{Vin} = 1$. Figure 15 shows the resulting circuit.

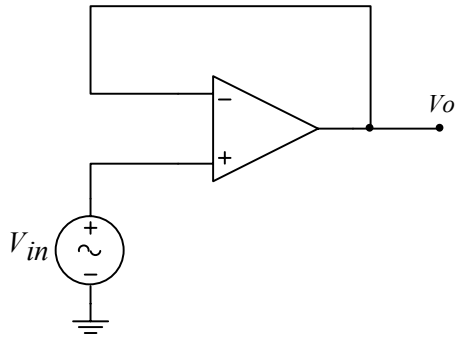


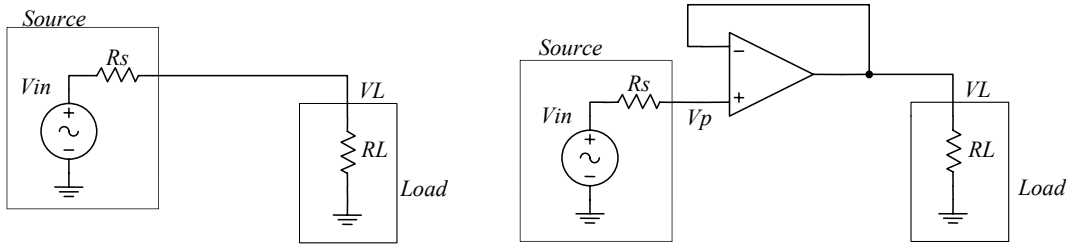
Figure 15. Voltage follower op-amp circuit

The voltage gain of this configuration is 1. The output voltage follows the input.

So what is the usefulness of this op-amp circuit?

Let's look at the input and output resistance characteristics of the circuit. As we have discussed, the resistance at the input terminals of the op-amp is very large. Indeed, for our ideal model we have taken the value of that resistance to be infinite. Therefore the signal *Vin* sees a very large resistance which eliminates any loading of the signal source. Similarly, since the output resistance of the op-amp is very small (zero ideally), the loading is also eliminated at the output of the device. In effect this is a resistance transformer.

In order to see the importance of this **buffer** circuit let's consider the case where the input signal is a source with an output resistance Rs and is connected to a load with resistance RL. In Figure 16(a) the signal source is connected directly to the load RL.



(a) (b)

Figure 16. (a) Source and load connected directly. (b) Source and load connected via a voltage follower.

From Figure 16(a), the voltage divider formed by Rs and RL gives a value for VL which is a fraction of Vin given by

$$VL = Vin\frac{RL}{RL + Rs} \tag{1.24}$$

For example, if $RL = 1k\Omega$ and $Rs = 10\ k\Omega$, then $VL \approx 0.1\ Vin$ which represents a considerable attenuation (loading) of the signal source.

If we now connect the signal source to the load with a buffer amplifier as shown on Figure 16(b). Since the input resistance of the amplifier is very large (no current flows into the terminal), the voltage at the non-inverting terminal, *Vp*, is equal to *Vin*. In addition, since the output resistance of the op-amp is zero, the voltage across the load resistor $VL = Vo = Vin$. The load now sees the input voltage signal but it places no demands on the signal source since it is "buffered" by the operational amplifier circuit.

Example: Non-Inverting amplifier design

Design an amplifier with a gain of 20dB by using standard 5% tolerance resistors. The input signal is in the range -1V to +1V. The amplifier is to drive a resistive load. For your design you may use an op-amp with the ability to deliver a maximum current of 100mA.

Standard 5% resistors are available with values from 10Ω to 10MΩ. The decade values can be found from the following table.

Table I. Standard 5% resistor values

10	11	12	13	15	16	18	20	22
24	27	30	33	36	39	43	47	51
56	62	68	75	82	91			

For example, if we consider the multiplier 11, the possible 5% resistor values corresponding to it are 11Ω, 110Ω, 1.1kΩ, 11kΩ, 110kΩ, 1.1MΩ. For other multipliers, the values may be found by following this example.

Solution:

The non-inverting amplifier circuit is

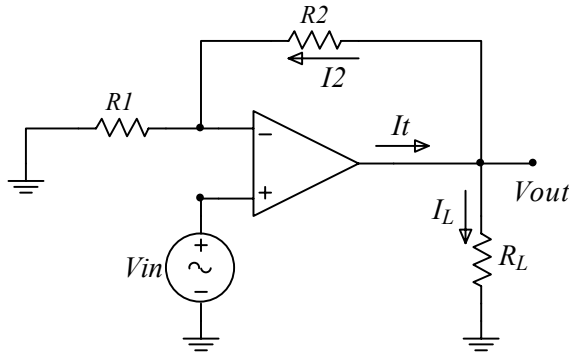


Figure 17. Amplifier circuit.

From the definition of dB we have: $20dB = 20\log\frac{V_{out}}{V_{in}}$ and so $\frac{V_{out}}{V_{in}} = 10$.

The closed loop gain is given by Equation (1.23) and thus for our design

$$10 = 1 + \frac{R2}{R1} \tag{1.25}$$

Our task is now to determine the values for *R1* and *R2* that satisfy the design constraints. We need two resistors whose ratio is 9 (*R2/R1 = 9*). From the values listed on the 5% table we have a few options. Some of our options are:

R2=180Ω and R1=20Ω
R2=1.8kΩ and R1=0.2kΩ
R2=18kΩ and R1=2kΩ
R2=180kΩ and R1=20kΩ
R2=1.8MΩ and R1=200kΩ

The power constraint will now guide us in determining the actual value of resistors *R1* and *R2*. With an input voltage of *+1V* the output voltage *Vo=10V* and thus the current *It* delivered by the op-amp must be less than 100mA.

If all the current is passing through resistor R_L then R_L is limited to *1kΩ*.

Besides the path through R_L current may also flow to ground through *R2* and *R1*. Since no current flows into the terminals of the op-amp, the fraction of the current that flows through *R2* and *R1* is

$$I2 = It\left(\frac{R1+R2}{RL+R1+R2}\right) \tag{1.26}$$

Note that if the resistance value of R_L is comparable to that of *R1+R2*, then a large fraction of the current provided by the op-amp flows through the feedback loop.

Therefore in order to tightly satisfy the current constraint of the op-amp we must also consider the amount of current that flows through the feedback loop. The table below shows some of the many design possibilities.

Table II. Possible designs

R_L	*R1*	*R2*	*IL*	*I2*	*It*
0.1kΩ	20Ω	180Ω	100mA	50mA	150mA
0.1kΩ	0.2kΩ	1.8kΩ	100mA	5mA	105mA
0.1kΩ	2kΩ	18kΩ	100mA	0.5mA	100.5mA
110Ω	*2kΩ*	*18kΩ*	*90.9mA*	*0.5mA*	*91.4mA*
110Ω	*20kΩ*	*180kΩ*	*90.9mA*	*0.05mA*	*90.95mA*
110Ω	*200kΩ*	*1.80MΩ*	*90.9mA*	*0.005mA*	*90.905mA*

If we consider the 5% tolerance of the resistors we conclude that we are limited to the following resistor values:

$$\left.\begin{array}{l} RL > 100\Omega \\ R1 \geq 2k\Omega \\ R2 \geq 18k\Omega \end{array}\right\} \qquad (1.27)$$

Any set of the values in the enclosed dotted box on Table II may be used in this design. In practice we should however avoid extremely large resistance values in the feedback circuit.

Problem:

Consider a signal source with a source output resistance *Rs* connected to the inverting amplifier as shown on Figure P2. Calculate the gain of the amplifier, assuming that the load cannot be ignored. Define the conditions for which the loading can be ignored.

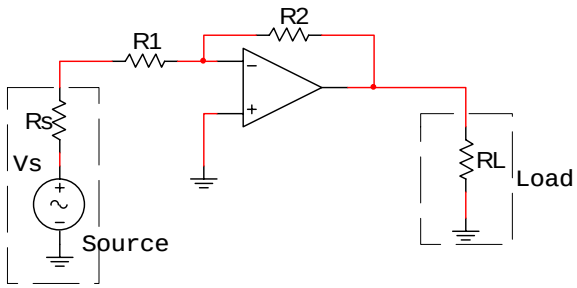


Figure P2

Input and Output Resistance of negative feedback circuits.

(Inverting and Non-Inverting Amplifiers)

As we saw in the example of the buffer amplifier, op-amp amplifier circuits may, besides voltage amplification, provide impedance transformation. It is thus important to be able to determine the input and the output resistance seen by a source or a load connected to an op-amp circuit.

The input impedance of an op-amp circuit with negative feedback may in general be very different from the open loop input/output resistance of an op-amp.

Input resistance

Inverting amplifier

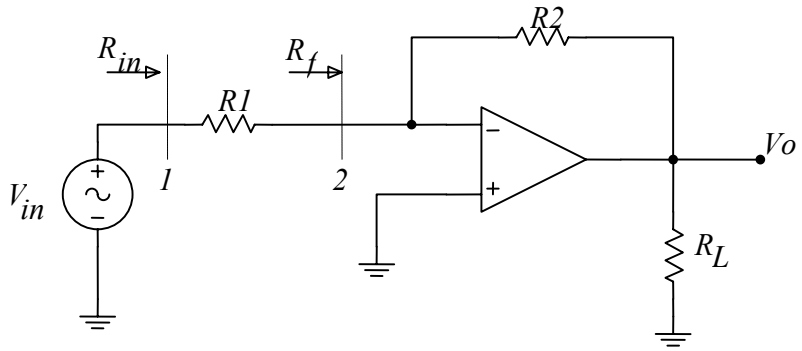


Figure 18. Inverting amplifier showing input resistance.

The input resistance of the inverting amplifier, or equivalently the resistance seen by the source *Vin*, is *Rin* as shown on Figure 18. By designating as *Rf*, the resistance to the right of point 2, we have *Rin = R1 + Rf*. Determining *Rf* and then adding *R1* for the total input resistance is an easier process than performing the calculation together.

The equivalent resistance *Rf* may be determined by considering the circuit shown on Figure 19(a). Here we apply a test current *It* and calculate the resulting voltage *Vt*. The resistance *Rf* is then given by *Rf=Vt/It.*

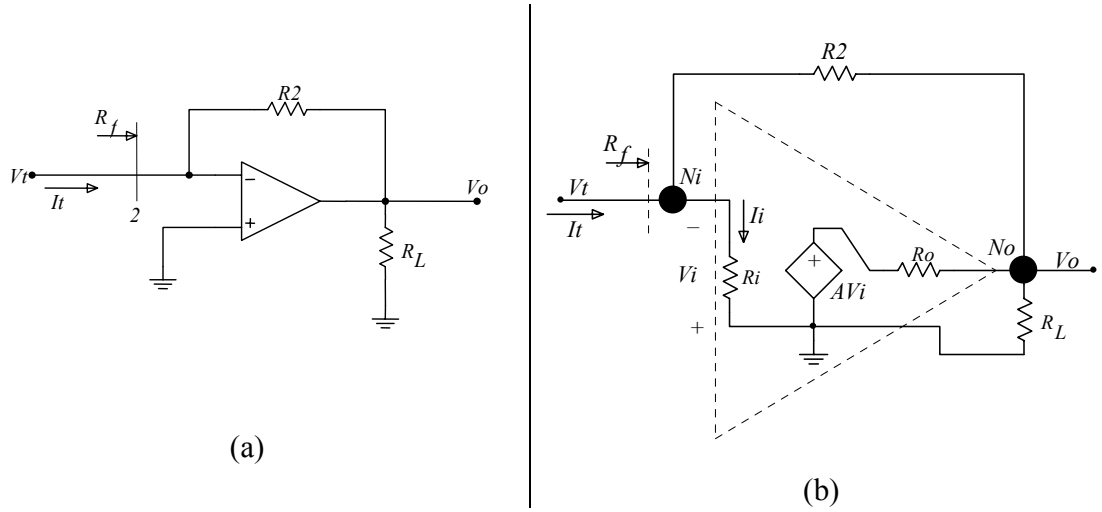


Figure 19. (a) Circuit for the calculation of the input resistance. (b) equivalent circuit for the calculation of input resistance R_f.

By considering the op-amp model with open loop gain *A*, input resistance *Ri* and output resistance *Ro*, the equivalent circuit of interest is shown on Figure 19(b). By applying KCl at the input and output nodes (*Ni* and *No*) we have:

KCL at node *Ni* gives:

$$I_t = \frac{V_t}{Ri} + \frac{V_t - Vo}{R2} \tag{1.28}$$

KCL at node *No* gives:

$$\frac{Vo}{RL} + \frac{Vo - \left(A\left(-V_t\right)\right)}{Ro} + \frac{Vo - V_t}{R2} = 0 \tag{1.29}$$

The ratio *Vt/It* may be obtained from Equations (1.28) and (1.29) by eliminating *Vo*. The input resistance of the inverting amplifier is,

$$\frac{1}{R_f} \equiv \frac{It}{Vt} = \frac{1}{R_i} + \frac{1}{R_2}\left[\frac{1 + A + \frac{R_o}{R_L}}{1 + \frac{R_o}{R_L} + \frac{R_o}{R_2}}\right] \tag{1.30}$$

In the ideal case where $A \to \infty$, the resistance $R_f \to 0$, implying that $Vt \to 0$ and $It \to 0$: the ideal op-amp rules.

For simplicity let's assume that *Ro=0*. Then,

$$\frac{1}{R_f} = \frac{1}{R_i} + \frac{1+A}{R_2} \tag{1.31}$$

For all practical situations $R_2 << R_i$ and Equation 16 gives:

$$R_f \cong \frac{1}{1+A} R_2 \tag{1.32}$$

Which shows that the input resistance R_f is a very strong function of the open loop gain and the input resistance of the op-amp, R_i, has a negligible effect on the resistance R_f.

For the 741 op-amp which has *A=200 V/mV,* R_i *= 2 MΩ* and R_o *= 100Ω* an inverting amplifier with *R2=10 kΩ*, is characterized by R_f *= 0.5 mΩ*. This is a negligible value for all applications of interest.

Therefore, the effective resistance seen by the source is $\approx R1$.

Non-inverting amplifier

Figure 20 shows the equivalent non-inverting amplifier circuit for the calculation of the input resistance R_{in}. We apply a test voltage Vt and calculate the resulting current It. The input resistance is then $R_{in}=Vt/It$.

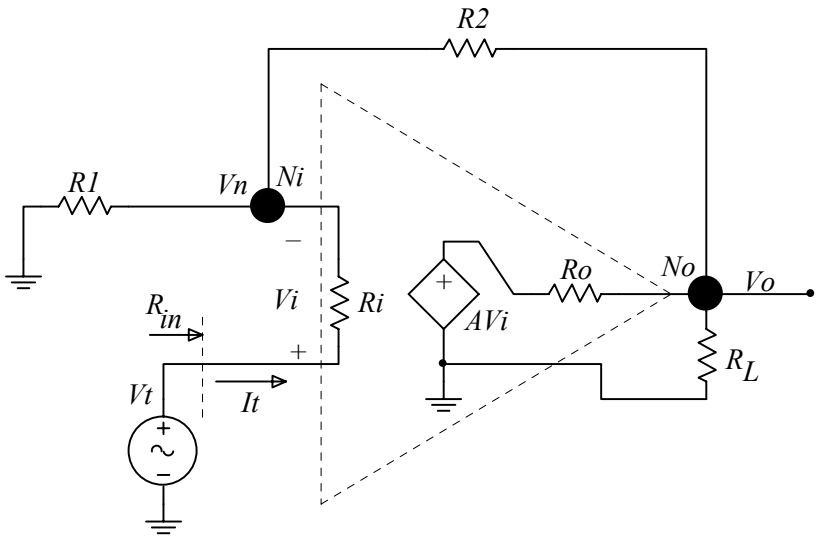


Figure 20. Non-inverting amplifier equivalent circuit for the calculation of the input resistance.

We proceed by applying KCL at nodes *Ni* and *No*.

KCL at node *Ni* gives:

$$It-\frac{Vn}{R1}-\frac{Vn-Vo}{R2}=0 \tag{1.33}$$

KCL at node *No* gives:

$$\frac{Vo}{RL}+\frac{Vo\ -\ \left(A\left(Vi\right)\right)}{Ro}+\frac{Vo\ -\ Vn}{R2}=0 \tag{1.34}$$

Since $Vi = Vt – Vn = I\,Ri$, Equations (1.33) and (1.34) after some algebraic manipulations give

$$\frac{Vt}{It}=Rin=\frac{1+\frac{Ro}{RL}+\frac{Ro}{R2}+\left[\left(\frac{1}{R1}+\frac{1}{R2}\right)\left(1+\frac{Ro}{RL}+\frac{Ro}{R2}\right)-\frac{Ro}{R2^2}+\frac{A}{R2}\right]Ri}{\left(\frac{1}{R1}+\frac{1}{R2}\right)\left(1+\frac{Ro}{RL}+\frac{Ro}{R2}\right)-\frac{Ro}{R2^2}} \tag{1.35}$$

For a simplification of the above expression let's neglect *Ro* which is anyway small compared to other values. Equation (1.35) now becomes

$$Rin = \frac{R2\left(1+\frac{Ri}{R1}\right)+Ri\left(1+A\right)}{1+\frac{R2}{R1}} \tag{1.36}$$

In the limit $A \to \infty$, $Rin \to \infty$. Similarly, in the limit $Ri \to \infty$, $Rin \to \infty$.

Output Resistance

The equivalent circuit for the calculation of the output resistance is shown on Figure 17. Note that this equivalent circuit, which is obtained by suppressing the input sources, is common for both the inverting and the non-inverting amplifiers. We apply a rest voltage V at the output and calculate the resulting current I. The output resistance is Rout=V/I.

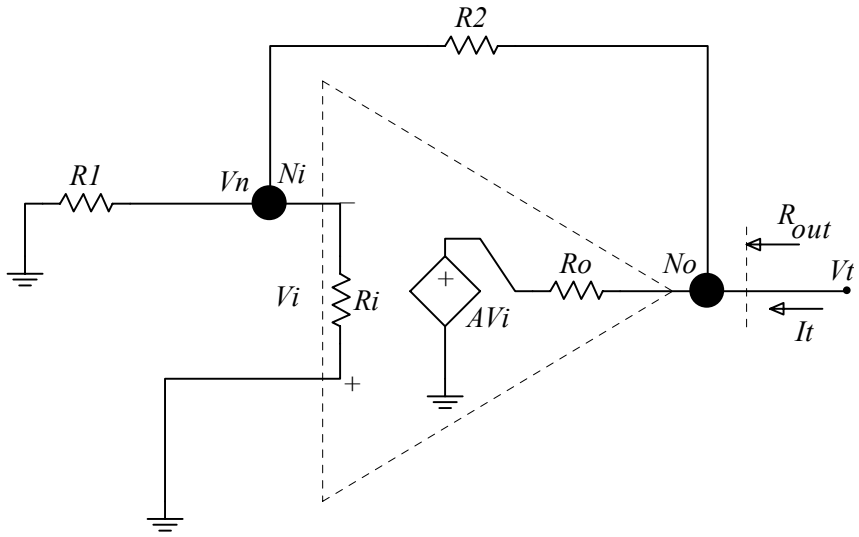


Figure 21. Model for the calculation of output resistance

KCL at node *No* gives:

$$I + \frac{-AVn - Vt}{Ro} + \frac{Vn - Vt}{R2} = 0 \tag{1.37}$$

By noting that resistors *R1* and *Ri* are in parallel, the voltage *Vn* at node *Ni* is

$$Vn = Vt \frac{\frac{R1Ri}{R1+Ri}}{\frac{R1Ri}{R1+Ri} + R2} \tag{1.38}$$

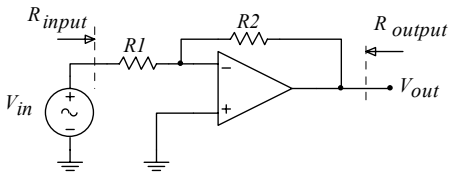
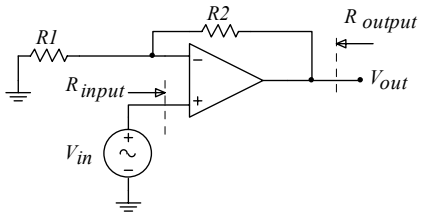
By substituting Equation (1.38) into Equation (1.37) the ratio *Vt/It* becomes

$$\frac{Vt}{It} = Rout = \frac{Ro\left(1 + \frac{R2}{R1} + \frac{R2}{Ri}\right)}{1 + \frac{R2}{R1} + \frac{R2}{Ri} + A + \frac{Ro}{R1} + \frac{Ro}{Ri}} \tag{1.39}$$

In typical circuits $R2 << Ri$, $Ro \cong 100\Omega$ and $A >> 1$. Therefore the output resistance is very small. For our typical 741 op-amp, with $Ro = 100\Omega$, $Ri = 2M\Omega$, and A=200V/mV, arranged as an inverting amplifier of gain -10 the output resistance is 5.5mΩ.

Table III summarizes the results for the input and output resistance of the ideal inverting and non inverting amplifiers. These general results are sufficient for the design of most amplifiers of interest. The non inverting amplifier is the most useful configuration in terms of its ideal coupling characteristics with the signal source. The signal source sees an infinite input resistance and thus the non-inverting amplifier places no loading demands on the source. Furthermore, the input resistance seen by the source does not change as the gain of the amplifier changes. By contrast, when a source is connected to an inverting amplifier, the source sees the resistor R1 as the input resistance of the amplifier.

Table III. Summary of ideal amplifier characteristics.

	Inverting amplifier	Non inverting amplifier
		
Gain: $\left(\frac{Vout}{Vin}\right)$	$-\frac{R2}{R1}$	$1+\frac{R2}{R1}$
Rinput	$R1$	∞
Routput	0	0

Practical op-amp considerations

Input Offset and Input Bias currents

For an ideal op amp no current flows into its input terminals. However, for real op amps there is a small amount of current that flows into the inverting and non inverting terminals as shown on Figure 22.

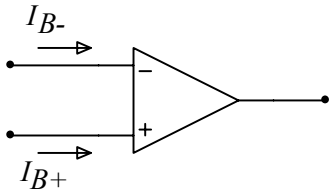


Figure 22. Op-amp symbol with input currents.

The electrical characteristics table of op-amp device data sheets give the values for Input offset current (I_{IO}) and the Input Bias current (I_{IB}), where I_{IO} and I_{IB} are defined by

$$I_{IO} = \left| I_{B+} - I_{B-} \right| \tag{1.40}$$

$$I_{IB} = \frac{I_{B+} + I_{B-}}{2} \tag{1.41}$$

In order to quantify the effect of the currents I_{B+} and I_{B-} lets consider the amplifier configuration of Figure 23 for which all inputs have been set to zero.

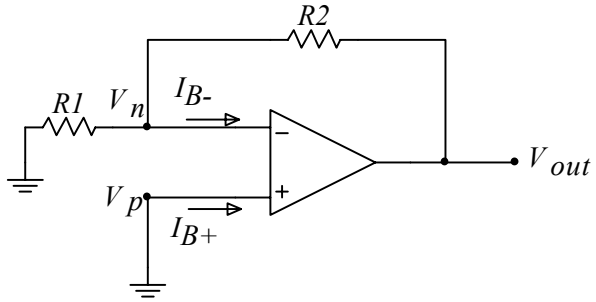


Figure 23. Amplifier for the evaluation of the effect of the input bias currents.

If I_{B+} and I_{B-} are zero then the output voltage V_{out} will also be zero.

The voltage error due to the bias currents I_{B+} and I_{B-} is generated by the flow of these currents through resistor *R2*. For the 741 op amp, the typical room temperature values for

I_{IO} and I_{IB} are: I_{IO}=*20 nA and* I_{IB}=*80 nA*. For an amplifier with R2=100kΩ, the resulting output voltage is $V_{out} = I_{B-}\ R2\ =\ (90nA)\ (100k\Omega)\ =\ 9\ mV$. In some application this might be an unacceptable value.

This "error" voltage may be reduced by simply selecting a smaller resistor *R2*. In some cases this might be sufficient assuming that other circuit characteristics like power consumption is not violated.

In general however the effect of the bias currents may be reduced by employing the appropriate "compensation technique." Such an arrangement is shown on Figure 24, where we have used resistor *Rp* at the non inverting terminal.

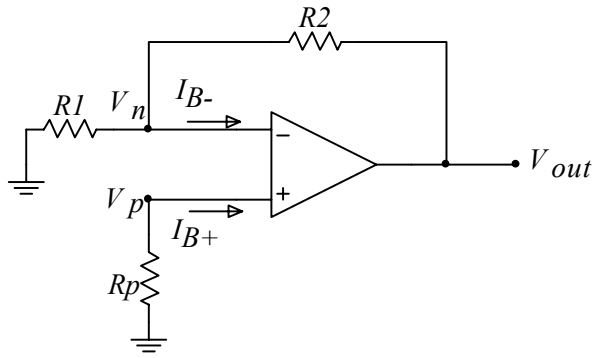


Figure 24. Amplifier circuit with bias current compensating resistor.

Since we have a linear system the effect of the bias currents on V_{out} can be estimated by using the principle of superposition. We have two cases:

1. $I_{B+} = 0$ which gives $V_{out(n)} = I_{B-}R2$
2. $I_{B-} = 0$ which gives $V_{out(p)} = \left(1+\frac{R2}{R1}\right)Vp\ =\ -\ \left(1+\frac{R2}{R1}\right)I_{B+}R3$

And superposition gives

$$Vout\ =\ I_{B-}R2\ -\ \left(1+\frac{R2}{R1}\right)I_{B+}R3 \qquad (1.42)$$

Before we proceed with further algebraic manipulation of Equation (1.42) let's look at the operation of the circuit.

The equivalent resistance of the feedback network seen at node *Vn* is the parallel combination of *R1* and *R2*. By further assuming that $I_{B+} = I_{B-}$, the desired system symmetry can be maintained if the resistance seen at node *Vp* is the same as that seen at node *Vn*. Therefore if *Rp* has a value that is equal to the parallel combination of *R1* and *R2* the differential voltage at the inputs of the op amp balances the effect of the input currents.

Now by manipulating Equation (1.42) for the general case when $I_{B+} \neq I_{B-}$ we obtain

$$Vout = \left(1+\frac{R2}{R1}\right)\left[\underbrace{\left(\frac{R1R2}{R1+R2}-Rp\right)I_{IB}}_{Bias\ Term} - \underbrace{\left(\frac{R1R2}{R1+R2}+Rp\right)\frac{I_{IO}}{2}}_{Offset\ Term}\right] \tag{1.43}$$

For $I_{B+} = I_{B-}$, $I_{IO}=0$ and the "*Offset Term*" of Equation (1.43) is zero. The "*Bias Term*" and thus V_{out} will then become zero when

$$Rp = \frac{R1R2}{R1+R2} \tag{1.44}$$

When $I_{B+} \neq I_{B-}$ and $Rp = R1 // R2 = \frac{R1R2}{R1+R2}$, the "*Bias Term*" becomes zero and V_{out} is

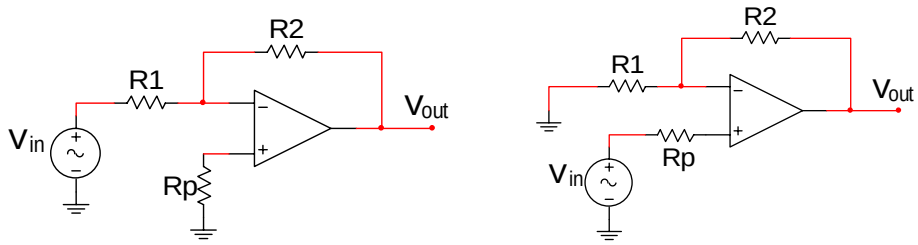
$$Vout = -\left(1+\frac{R2}{R1}\right)\left(\frac{R1R2}{R1+R2}+Rp\right)\frac{I_{IO}}{2} = -R2\ I_{IO} \tag{1.45}$$

The output error is thus proportional to the input offset current which for most op-maps is about an order of magnitude less than the currents I_{B+} and I_{B-}. For the 741 op amp $I_{B+} = 90nA$ and I_{IO}=20nA.

Design Practice (principle)

Always use a resistor Rp from the non inverting input to ground. Make

$$Rp = \frac{R1R2}{R1+R2}$$ Since we want the resistance seen by V- and V+ to be the same.



Input Offset Voltage

Besides the offset current at the inputs there also exists a nonzero difference voltage *Vi* at the input terminals even if we apply the same external voltage inputs. For the circuit of Figure 25 the out put voltage is not zero even though the input pins are grounded. The presence of this error voltage is due to transistor matching issues in the internal op-amp circuit.

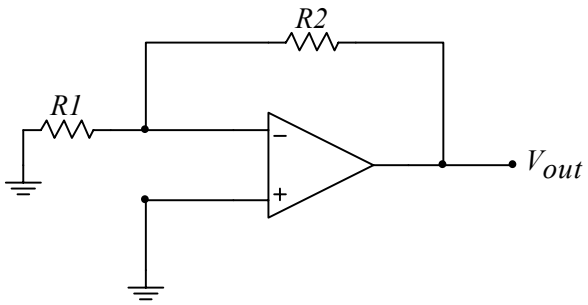


Figure 25. Output offset voltage

In the above figure, *Vo = Voff·(R1+R2)/R1*.

Common Mode Rejection Ratio (CMRR)

As we have seen, the usefulness of the op amp is derived from its ability to amplify differential signals. In fact the ideal op amp has an infinite gain for differential voltage signals. It is desired that signals that are common to both inputs "Common Mode (CM) Signals" be rejected by the amplifier. An ideal op amp has the ability to completely reject those CM signals; thus having infinite Common Mode Rejection (CMR) ability.

For an amplifier subjected to a differential voltage V_D and a common mode voltage V_{CM}, the output voltage is

$$Vo = G_D V_D + G_{CM} V_{CM} \tag{1.46}$$

Where G_D is the differential gain and G_{CM} is the common mode gain of the amplifier. In practice we would like to minimize G_{CM}. The ability of an amplifier to reject the CM signal is expressed by a parameter called the Common Mode Rejection Ratio (CMRR) which is defined as the ratio of the differential gain to common mode gain as follows.

$$\text{CMRR} \equiv 20 \log_{10} \left| \frac{\text{Gain of Differential Signal}}{\text{Gain of Common Mode Signal}} \right| = 20 \log_{10} \left| \frac{G_D}{G_{CM}} \right| \tag{1.47}$$

In the open loop configuration, our standard 741 op amp is characterized by a CMRR of 90dB for signal frequencies less than 100 Hz. At higher frequencies CMRR degrades considerably falling to 40dB at 100 kHz.

In general CMRR is not of concern in the inverting amplifier configuration. Can you see why? explain

Design Principle

Signal frequency is a fundamental parameter that drives circuit design

To see the effects of CMRR, drive a unity gain non-inverting 741 op-amp with a 10V step function; the output should be off 10V by a few hundred microvolts. This error is partially due to the finite open-loop gain of the op-amp and partially due to the CMRR. The inverting configuration leads to minimal common mode error since the amplifier's inputs are both at ground.