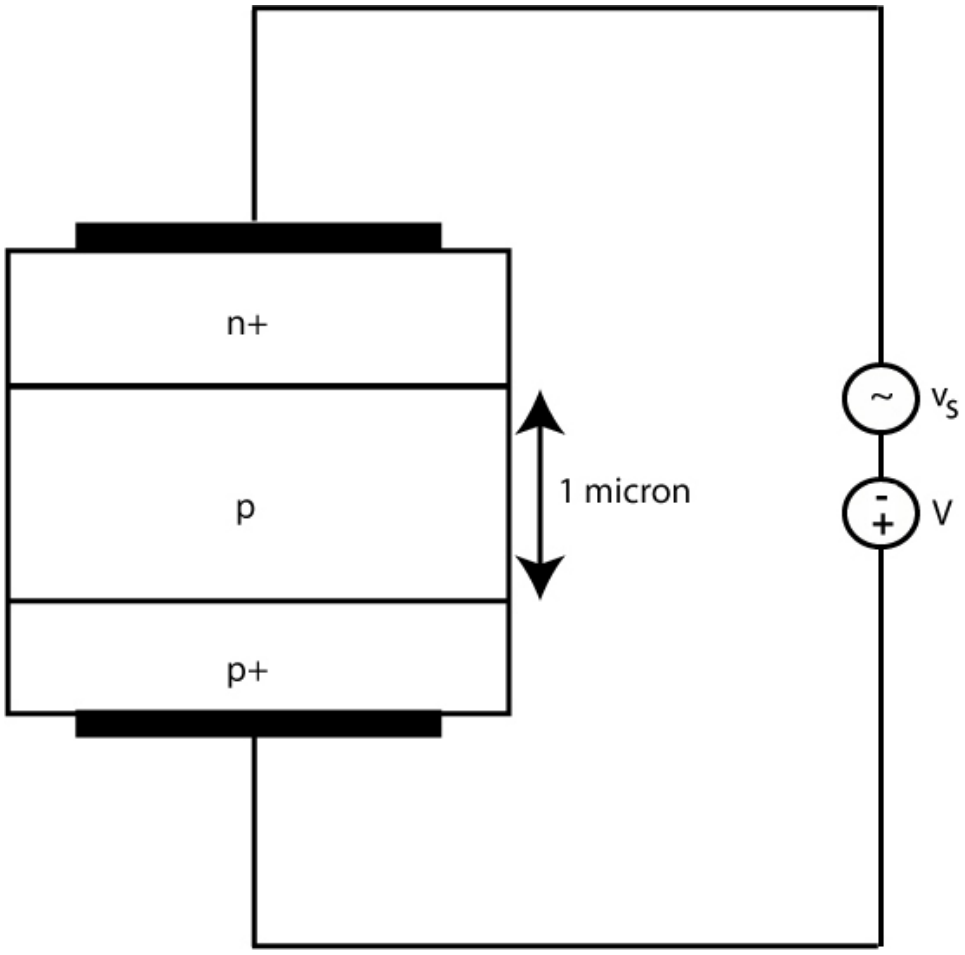
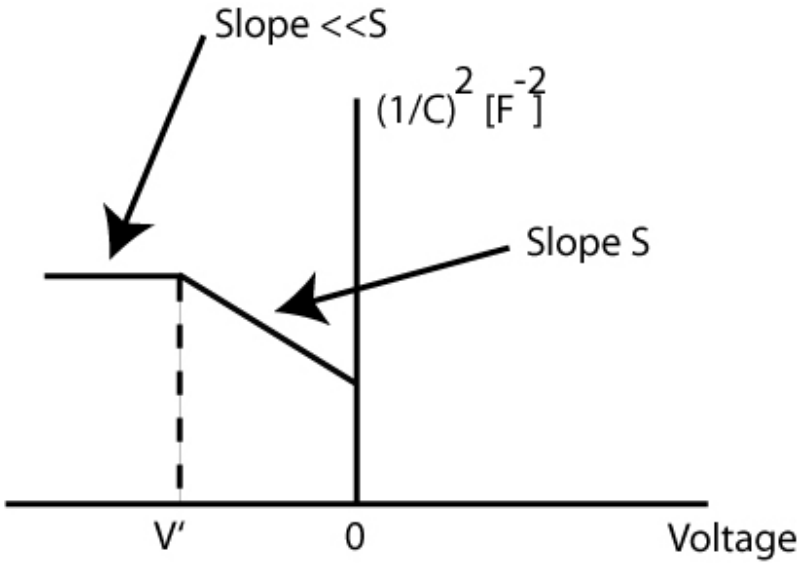
Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.012 Microelectronic Devices and Circuits
Homework #3

Problem 1 (10 points)

The device drawn below is biased as shown, and a capacitance-voltage (C-V) measurement is taken. The area of the device is 10^{-6} cm^2. Assume the electrostatic potential in the n+ silicon region, φ_{n+}=550mV.

A plot of $(1/C)^2$ as a function of the DC voltage, V, where C is the capacitance is shown below. The device is in reverse bias. The slope, S, is $-5 * 10^{26}$ F^{-2} V^{-1}.
NOTE: The polarity of the DC source is shown correctly.

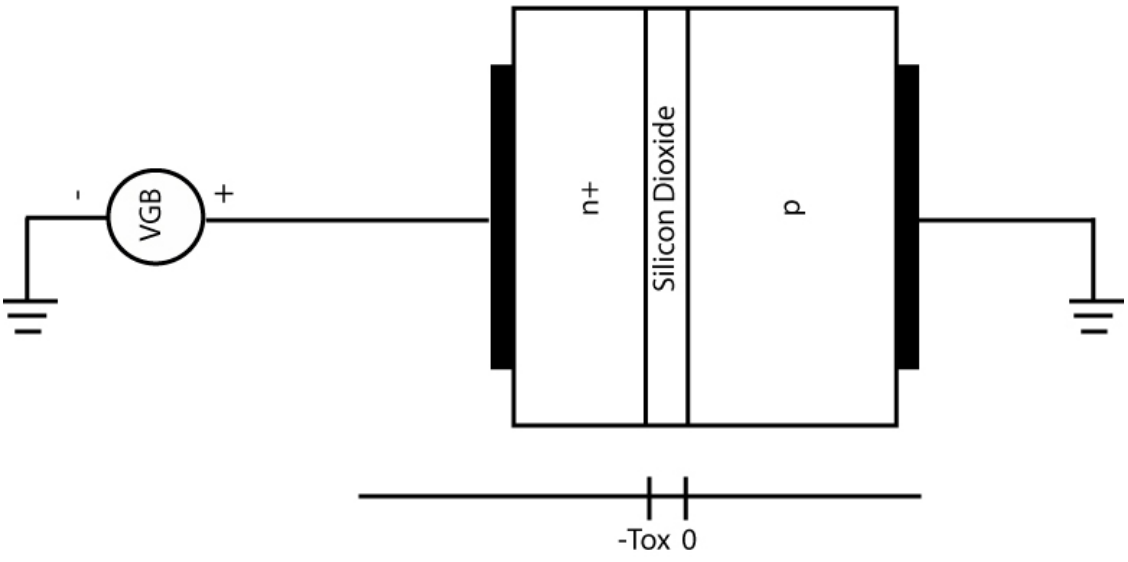




a) Derive an expression for the doping, N_a, in the p-type region in terms of the slope S, shown in the plot, and other known parameters (e.g. constants like q, ε_{Si}, the device area).
b) Assume now that N_a is 10^{17} cm^{-3}. Estimate the DC voltage V' where the slope of the plot of $(1/C)^2$ vs. voltage changes, as seen in the graph.

Problem 2 (35 points)

A metal-oxide-semiconductor (MOS) device is pictured below. T_{ox} is 15nm. Assume φ_{n+}=0.55V, and that N_a in the p region is 10^{16} cm^{-3}.



a) Find V_{FB}, V_{Tn}, X_{do}, φ_{so}.

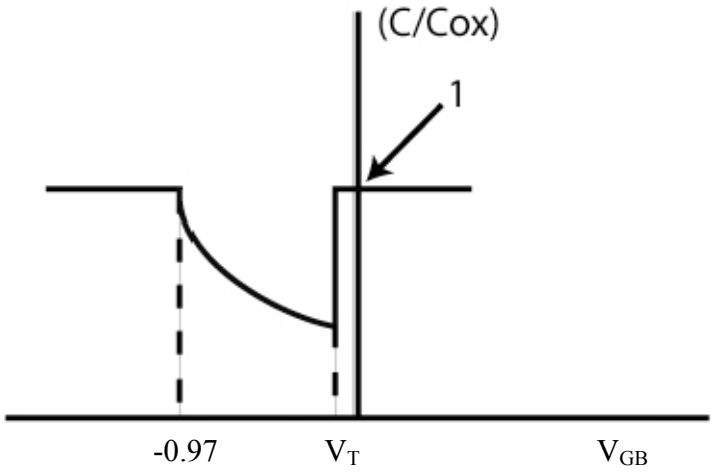
b) Find $X_{d,max}$.

c) Sketch $\varphi(x)$ for V_{GB}=0, -2V, and +2V from the n^+ gate through the oxide and into the silicon. Identify the regions of operation on the graph for each case of V_{GB}. You don't have to calculate φ_s for each case, but clearly show X_{do} and $X_{d,max}$ on the graph.

d) Plot the gate charge Q_G, as a function of V_{GB}, for V_{GB} ranging from -2 to 2 Volts. Identify the regions of operation on the graph and show how the slope changes in each region. Also, plot the capacitance of the structure over the same range. Calculate and label C_{min} and C_{max}.

Problem 3 (20 points)

Shown below is a capacitance-voltage plot for an MOS capacitor. The gate is n+, therefore you can assume its potential is 550mV. The silicon dioxide thickness is 15nm, and the body is doped with some concentration of acceptors, N_a.



a) Determine the flatband voltage, V_{FB}, on the C-V plot.

b) Calculate V_T. Hint: You will need to determine N_a first.

c) Specify the range of voltages where the MOS capacitor is in inversion, depletion, and accumulation.

d) Now assume the gate is doped p+, so the potential of the gate is -550mV. Sketch the C-V, labeling V_T and V_{FB}.

Problem 4 (5 points)

It is sometimes useful in analog circuits to use a transistor biased in triode as a voltage controlled resistor. Use the following parameters to design a n-channel MOSFET with a resistance of 10KΩ.
$\mu_n Cox=50\mu A/V^2$ $V_{Tn}= 1V$ $V_{GS}=1.5V$ $V_{BS}=0V$

a) If the device has a width of 10μm, what is the necessary length?

b) What is the necessary width to get a 1KΩ resistor, if the length is 5μm?

Problem 5 (10 points)

Hafnium dioxide (HfO_2, $\varepsilon= 25$) is an attractive replacement for silicon dioxide as a gate dielectric due to its high dielectric constant.

Consider a p-channel MOSFET. The channel length, L = 1μm, the width, W = 10μm, the hole mobility is $\mu_p = 150\ cm^2V^{-1}s^{-1}$ and the substrate doping is $N_d = 10^{17}cm^{-3}$. Assume the gate is p+ silicon, so its potential is -550mV.

a) What thickness of HfO_2 is needed for $V_{Tp} = -0.5$ V?

b) Find the backgate effect parameter, γ_p for the hafnium dioxide gate insulator thickness from (a).

c) If I=25μA, what is V_{SG}? Assume saturation.

d) What is the minimum drain voltage for saturation given V_{SG} calculated in (c)?

Problem 6 (10 points)

Howe and Sodini – P4.2

Problem 7 (10 points)

Howe and Sodini – P4.3

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