Lecture 19 - Differential Amplifier Stages - Outline

Announcements

Design Problem - coming out tomorrow; PS #10 looks at pieces; neglect the Early effect in large signal analyses

Review - Single-transistor building block stages

Common source: general purpose gain stage, workhorse

Common gate: small R_{in}, large R_{out}, unity A_i, same A_v as CS

Source follower: large R_{in}, small R_{out}, unity A_v, same A_i as CS

Series and Shunt feedback: we'll see in special situations

Differential Amplifier Stages - Large signal behavior

General features: symmetry, inputs, outputs, biasing **(Symmetry is the key!)**

Large signal transfer characteristic

Difference- and common-mode signals

Decomposing and reconstructing general signals

Half-circuit incremental analysis techniques

Linear equivalent half-circuits

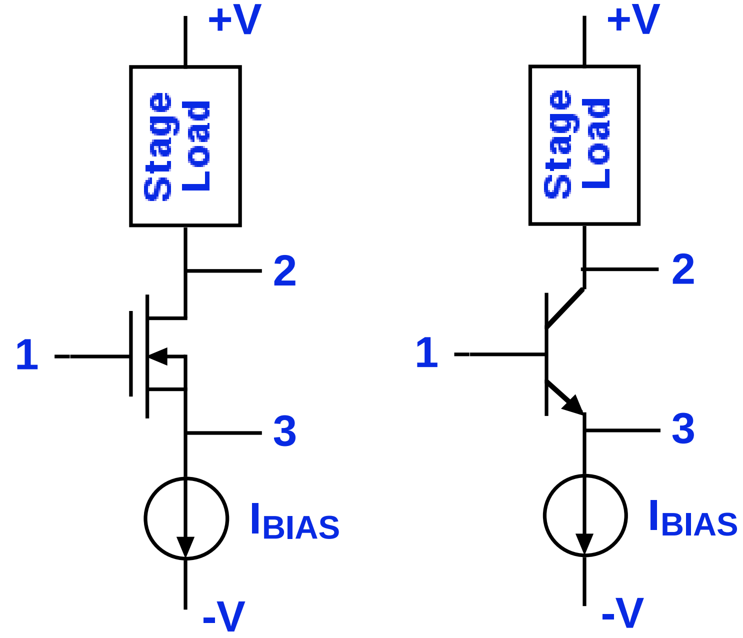
Difference- and common-mode analysis

Example: analysis of source-coupled pair

Linear amplifier layouts: The practical ways of putting inputs to, and taking outputs from, transistors to form linear amplifiers

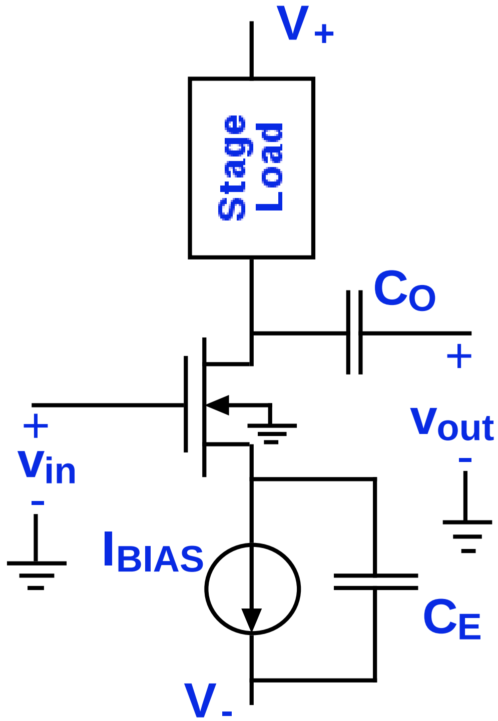
There are 12 choices: three possible nodes to connect to the input, and for each one, two nodes from which to take an output, and two choices of what to do with the remaining node (ground it or connect it to something).

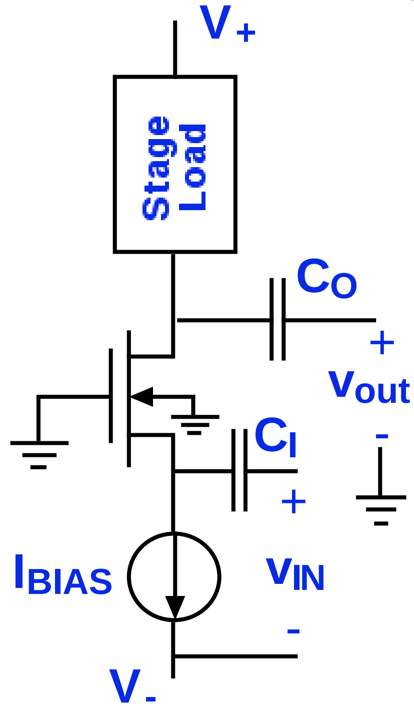
Not all these choices work well, however. In fact only three do:

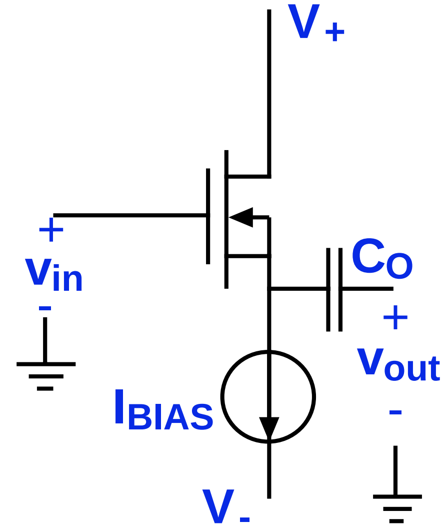


Name	Input	Output	Grounded
Common source/emitter	1	2	3
Common gate/base	3	2	1
Common drain/collector (Source/emitter follower)	1	3	2
Source/emitter degeneration	1	2	none

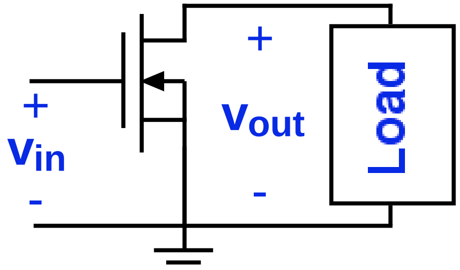
- **Three MOSFET single-transistor amplifiers**



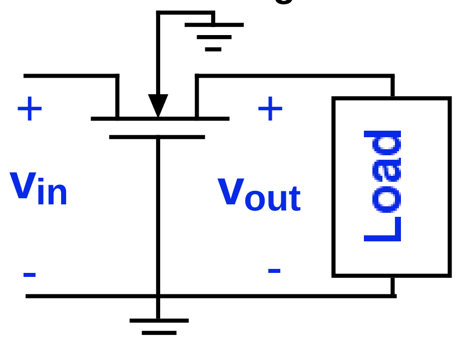




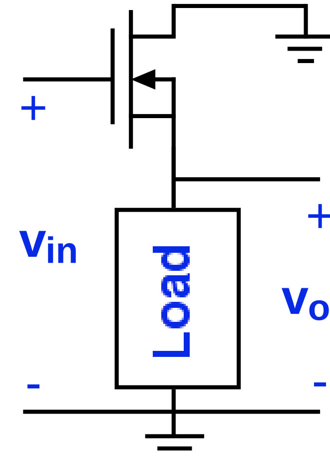
COMMON SOURCE
Input: gate
Output: drain
Common: source
Substrate: to source



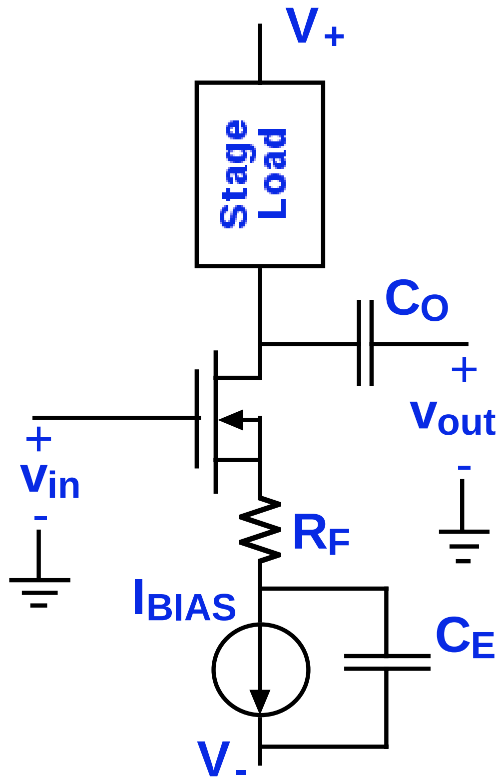
COMMON GATE
Input: source; Output: drain
Common: gate
Substrate: to ground

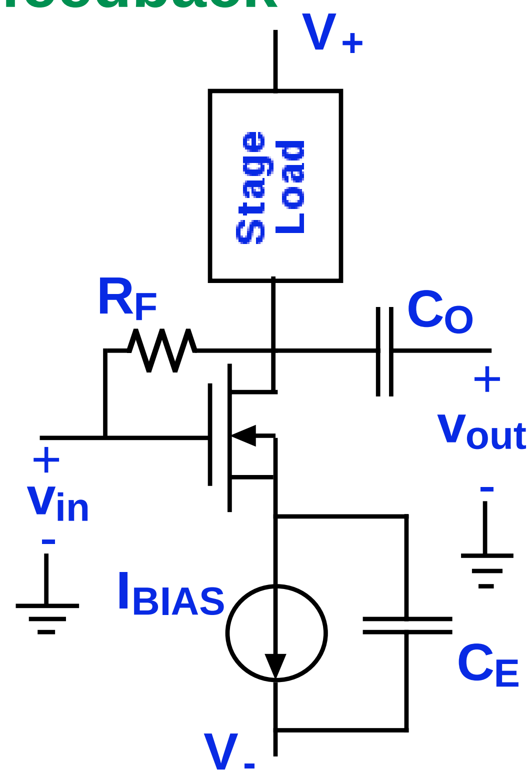


SOURCE FOLLOWER
Input: gate
Output: source
Common: drain
Substrate: to source



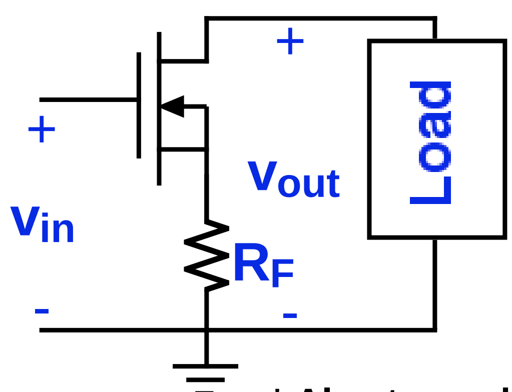
- **Single-transistor amplifiers with feedback**

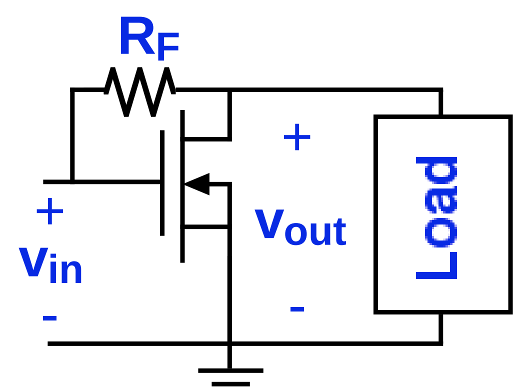




PARALLEL FEEDBACK*

SERIES FEEDBACK





* Also termed "source degeneracy"

- **Summary of the single transistor stages (MOSFET)**

MOSFET	Voltage gain, A_v	Current gain, A_i	Input resistance, R_i	Output resistance, R_o
Common source	$-\frac{g_m}{[g_o + g_l]} \left(= -g_m r_l'\right)$	∞	∞	$r_o \left(= \frac{1}{g_o}\right)$
Common gate	$\approx [g_m + g_{mb}]\, r_l'$	≈ 1	$\approx \frac{1}{[g_m + g_{mb}]}$	$\approx r_o \left\{1 + \frac{[g_m + g_{mb} + g_o]}{g_t}\right\}$
Source follower	$\frac{[g_m]}{[g_m + g_{mb} + g_o + g_l]} \approx 1$	∞	∞	$\frac{1}{[g_m + g_o + g_l]} \approx \frac{1}{g_m}$
Source degeneracy (series feedback)	$\approx -\frac{r_l}{R_F}$	∞	∞	$\approx r_o$
Shunt feedback	$-\frac{[g_m - G_F]}{[g_o + G_F]} \approx -g_m R_F$	$-\frac{g_l}{G_F}$	$\frac{1}{G_F[1 - A_v]}$	$r_o \parallel R_F \left(= \frac{1}{[g_o + G_F]}\right)$

Power gain, $A_p = A_v \cdot A_i$

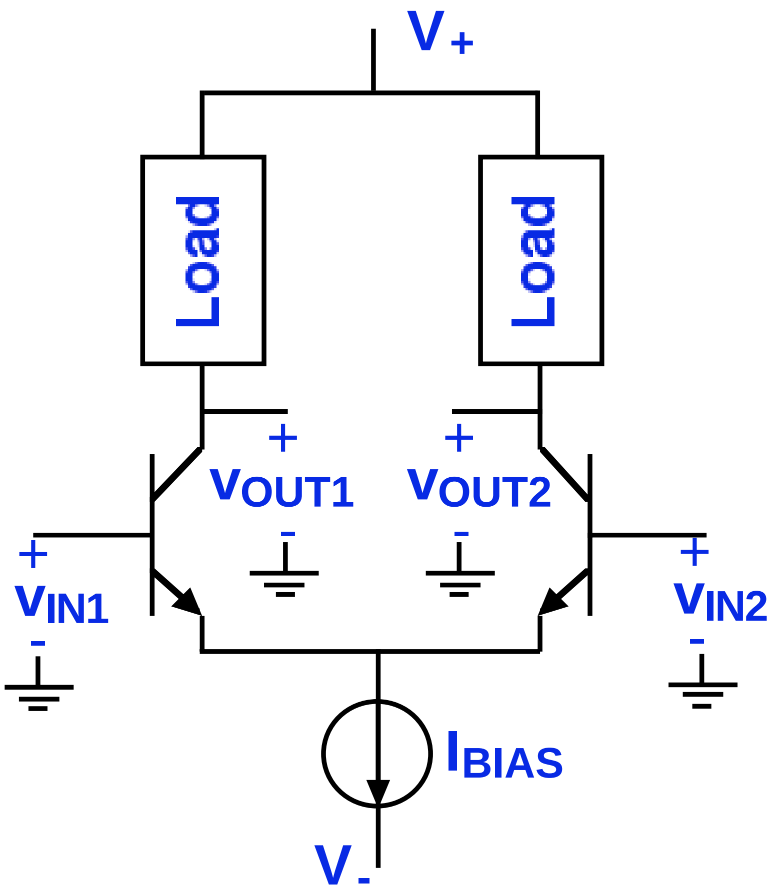
Note: When $v_{bs} = 0$ the g_{mb} factors should be deleted.

- **Summary of the single transistor stages (bipolar)**

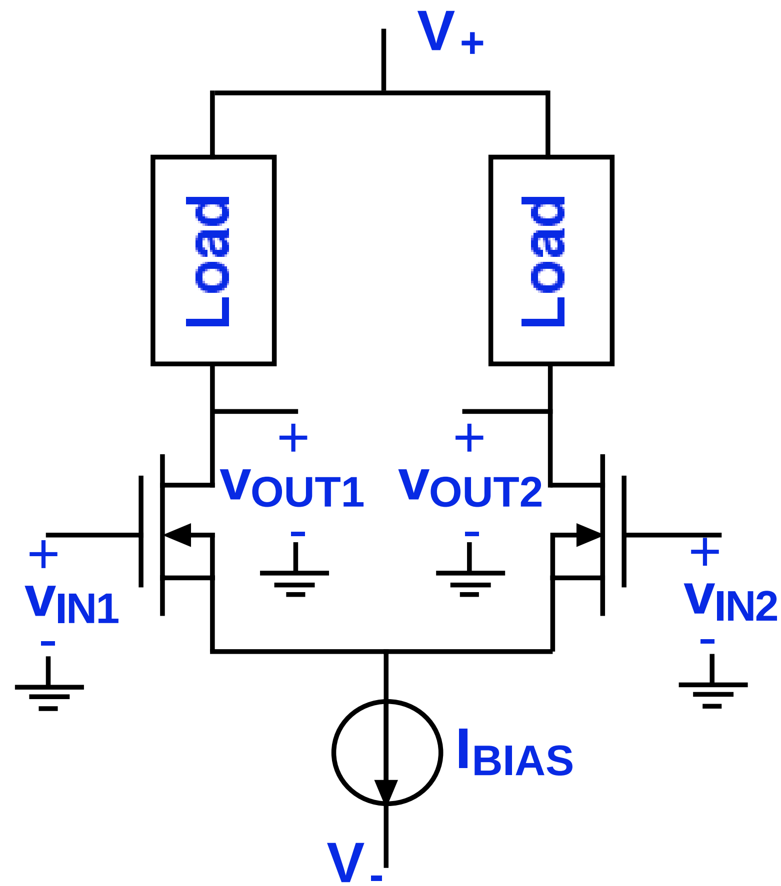
BIPOLAR	Voltage gain, A_v	Current gain, A_i	Input resistance, R_i	Output resistance, R_o
Common emitter	$-\frac{g_m}{[g_o + g_l]} \left(= -g_m r_l'\right)$	$-\frac{\beta\, g_l}{[g_o + g_l]}$	r_π	$r_o \left(= \frac{1}{g_o}\right)$
Common base	$\frac{g_m}{[g_o + g_l]} \left(= g_m r_l'\right)$	≈ 1	$\approx \frac{r_\pi}{[\beta + 1]}$	$\approx [\beta + 1] r_o$
Emitter follower	$\frac{[g_m + g_\pi]}{[g_m + g_\pi + g_o + g_l]} \approx 1$	$\frac{\beta\, g_l}{[g_o + g_l]} \approx \beta$	$r_\pi + [\beta + 1] r_l'$	$\frac{r_t + r_\pi}{[\beta + 1]}$
Emitter degeneracy	$\approx -\frac{r_l}{R_F}$	$\approx \beta$	$\approx r_\pi + [\beta + 1] R_F$	$\approx r_o$
Shunt feedback	$-\frac{[g_m - G_F]}{[g_o + G_F]} \approx -g_m R_F$	$-\frac{g_l}{G_F}$	$\frac{1}{g_\pi + G_F [1 - A_v]}$	$r_o \parallel R_F \left(= \frac{1}{g_o + G_F}\right)$

Power gain, $A_p = A_v \cdot A_i$

Differential Amplifiers: emitter- and source-coupled pairs



Emitter-coupled pair



Source-coupled pair

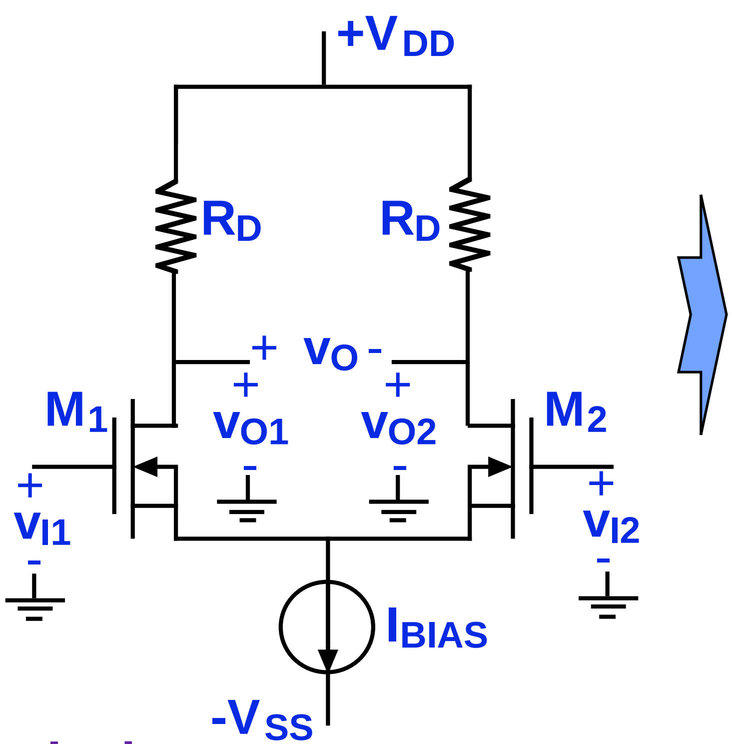
Why do we care? - They amplify only difference-mode signals
They are easy to interconnect and cascade
They help us eliminate coupling capacitors
They are optimally suited to integration

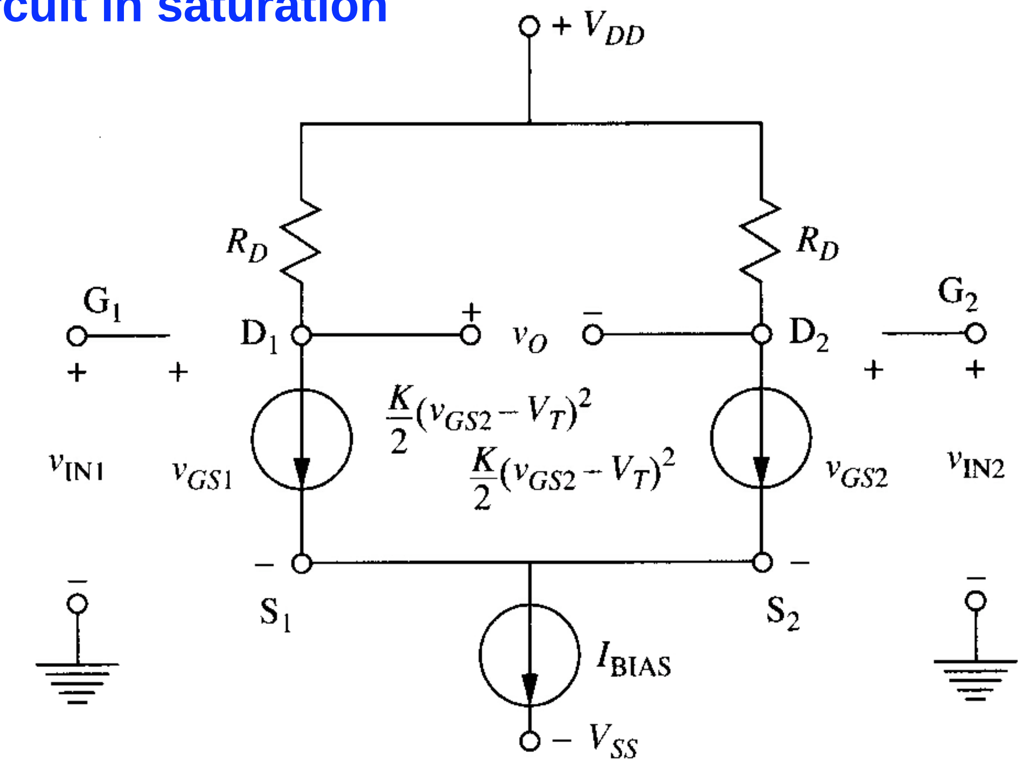
Differential Amplifiers: large signal analysis of source coupled pairs

Source-coupled pair

Below: Schematic with resistor loads

Right: Large signal equiv. circuit in saturation





Analysis:

3 KVL loops: $v_{I1} - v_{GS1} + v_{GS2} - v_{I2} = 0$, $v_{O1} = V_{DD} - R_D i_{D1}$, $v_{O2} = V_{DD} - R_D i_{D2}$

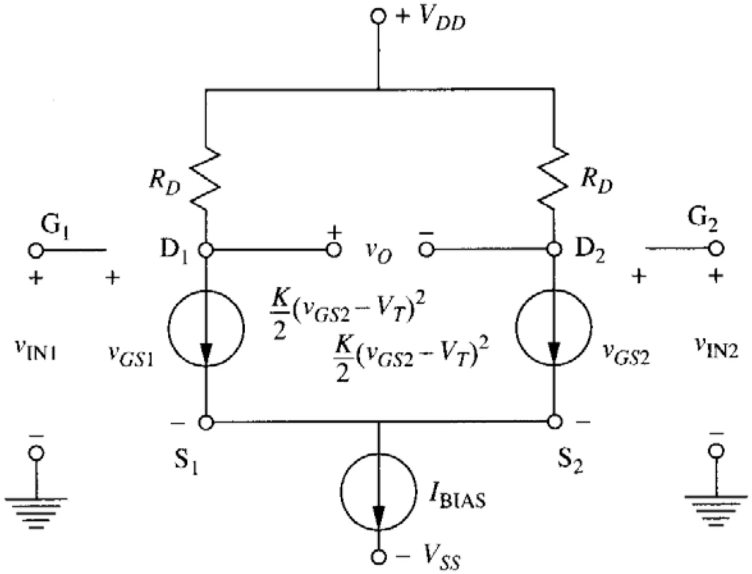
KCL at one node: $i_{D1} + i_{D2} = I_{BIAS}$

MOSFET relationships: $i_{D1} = K(v_{GS1}-V_T)^2/2$; $i_{D2} = K(v_{GS2}-V_T)^2/2$

(see text for details of analysis)

Diff. Amps: large signal analysis of source coupled pairs, cont.

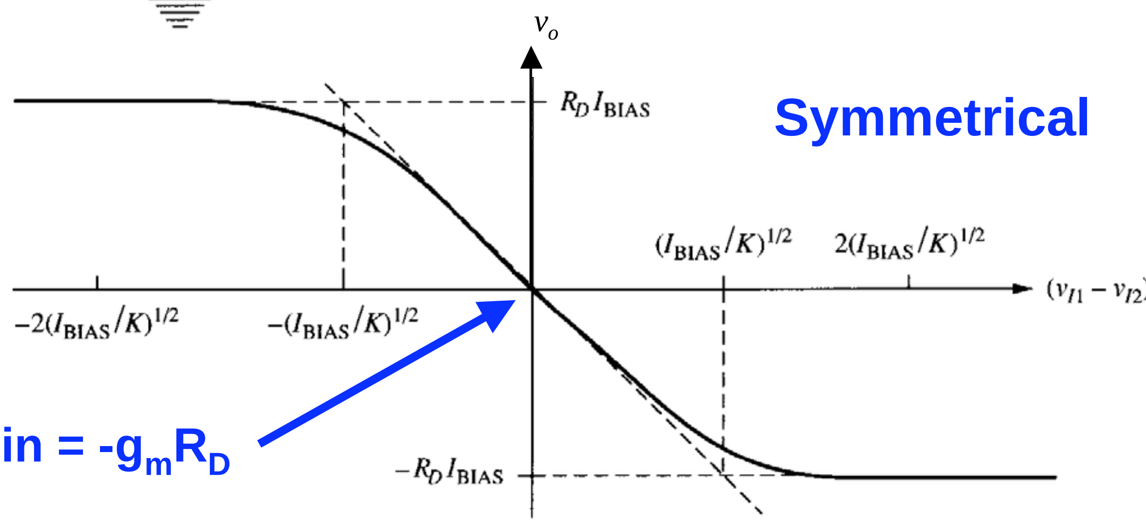
Results: The outputs again only depend on the difference between the two inputs, $(v_{I1} - v_{I2})$:



$$v_{O1} = V_{DD} - \frac{R_D}{2}\left\{ K[v_{IN1} - v_{IN2}]^2 + I_{BIAS} + \frac{K}{2}[v_{IN1} - v_{IN2}]\sqrt{\frac{4I_{BIAS}}{K} - [v_{IN1} - v_{IN2}]^2} \right\}$$

$$v_{O2} = V_{DD} - \frac{R_D}{2}\left\{ K[v_{IN1} - v_{IN2}]^2 + I_{BIAS} - \frac{K}{2}[v_{IN1} - v_{IN2}]\sqrt{\frac{4I_{BIAS}}{K} - [v_{IN1} - v_{IN2}]^2} \right\}$$

$$v_O = -\frac{R_D K}{2}[v_{IN1} - v_{IN2}]\sqrt{\frac{4I_{BIAS}}{K} - [v_{IN1} - v_{IN2}]^2}$$



Symmetrical

Slope around origin = $-g_m R_D$

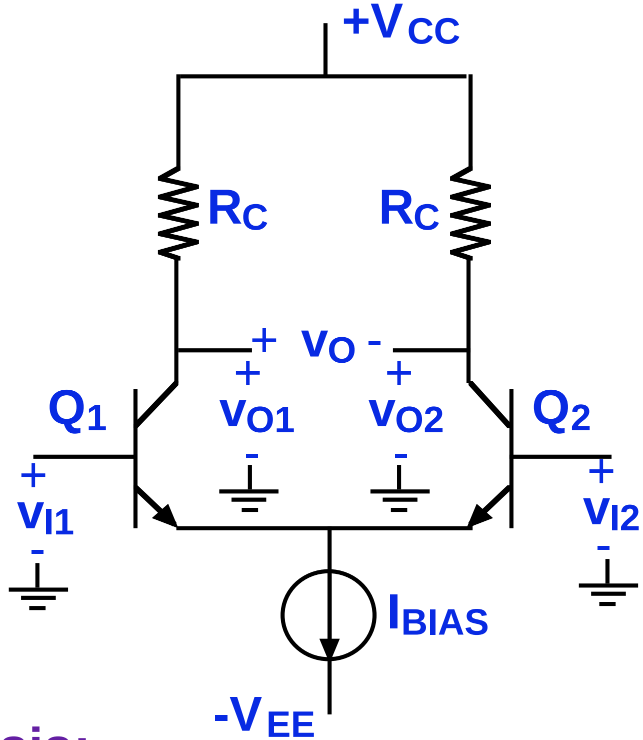
Only the difference in the inputs matters!!

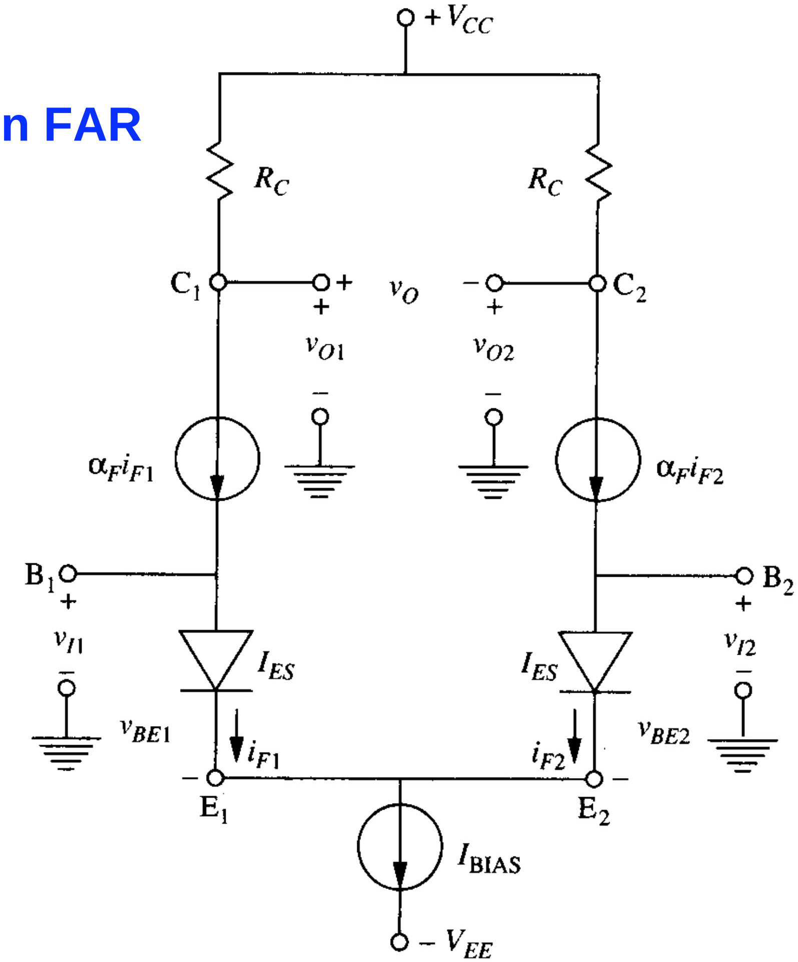
Differential Amplifiers: large signal analysis of emitter coupled pairs

Emitter-coupled pair

Below: Schematic with resistor loads

Right: Large signal equivalent circuit in FAR





Analysis:

3 KVL loops: $v_{I1} - v_{BE1} + v_{BE2} - v_{I2} = 0$, $v_{O1} = V_{CC} - R_C\alpha_F i_{F1}$, $v_{O2} = V_{CC} - R_C\alpha_F i_{F2}$

KCL at one node: $i_{F1} + i_{F2} = I_{BIAS}$

Ideal diode relationships: $i_{F1} \approx I_{ES} \exp(qv_{BE1}/kT)$, $i_{F2} \approx I_{ES} \exp(qv_{BE2}/kT)$

(see text for details of analysis)

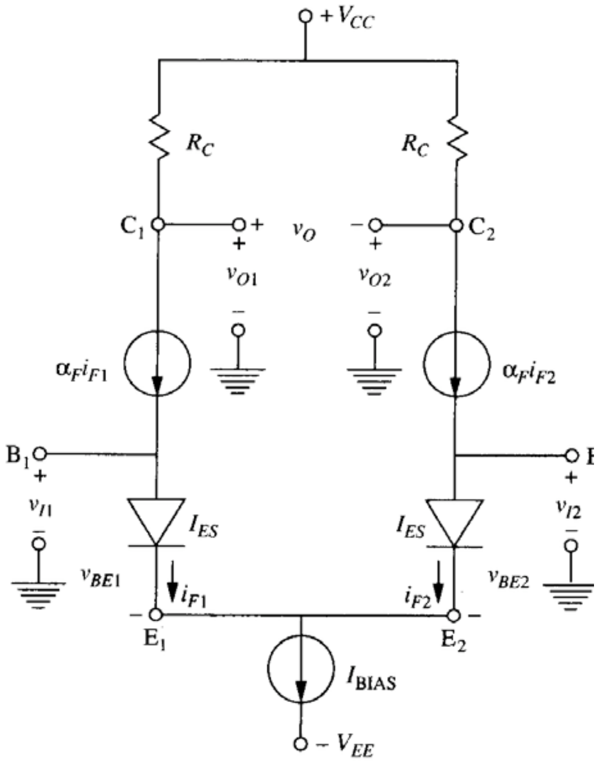
Diff. Amps: large signal analysis of emitter coupled pairs, cont.

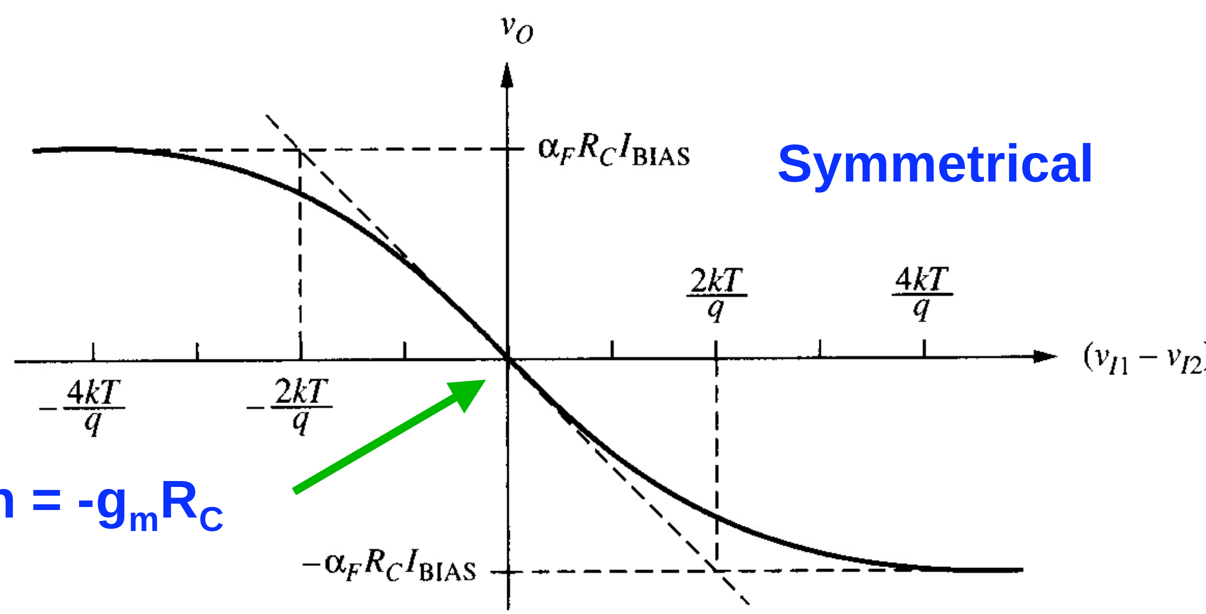
Results: The outputs only depend on the difference between the inputs, $(v_{I1} - v_{I2})$:

$$v_{O1} = V_{CC} - \frac{\alpha_F R_C I_{BIAS}}{\left[1 + e^{-q(v_{I1} - v_{I2})/kT}\right]}$$

$$v_{O2} = V_{CC} - \frac{\alpha_F R_C I_{BIAS}}{\left[1 + e^{q(v_{I1} - v_{I2})/kT}\right]}$$

$$v_O = -\alpha_F R_C I_{BIAS} \tanh \frac{q(v_{I1} - v_{I2})}{2kT}$$





Symmetrical

Slope around origin = $-g_m R_C$

Only the difference in the inputs matters!!

Differential Amplifier Analysis - difference-mode and common-mode signals

Any pair of signals can be decomposed into a portion that is the identical in both, and a portion that is equal, but opposite in both. For example, if we have two voltages, v_1 and v_2, we can define a common-mode signal, v_C, and a difference-mode signal, v_D, as:

$$v_C = (v_1 + v_2)/2 \qquad v_D = v_1 - v_2$$

In terms of these two voltages, we can write v_1 and v_2 as:

$$v_1 = v_C + v_D/2 \qquad v_2 = v_C - v_D/2$$

In incremental analysis of linear amplifiers we will decompose our inputs into difference- and common-mode inputs:

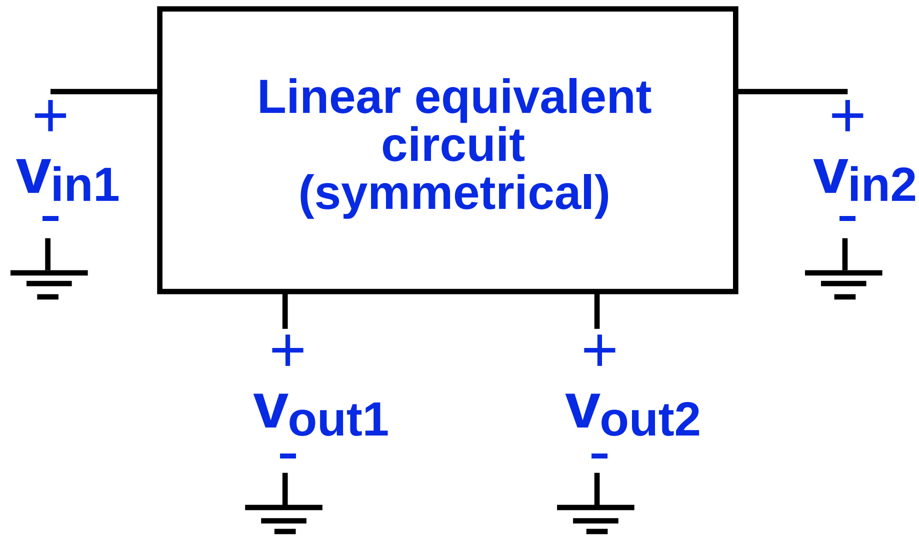
$$v_{ic} = (v_{in1} + v_{in2})/2 \text{ and } v_{id} = v_{in1} - v_{in2}.$$

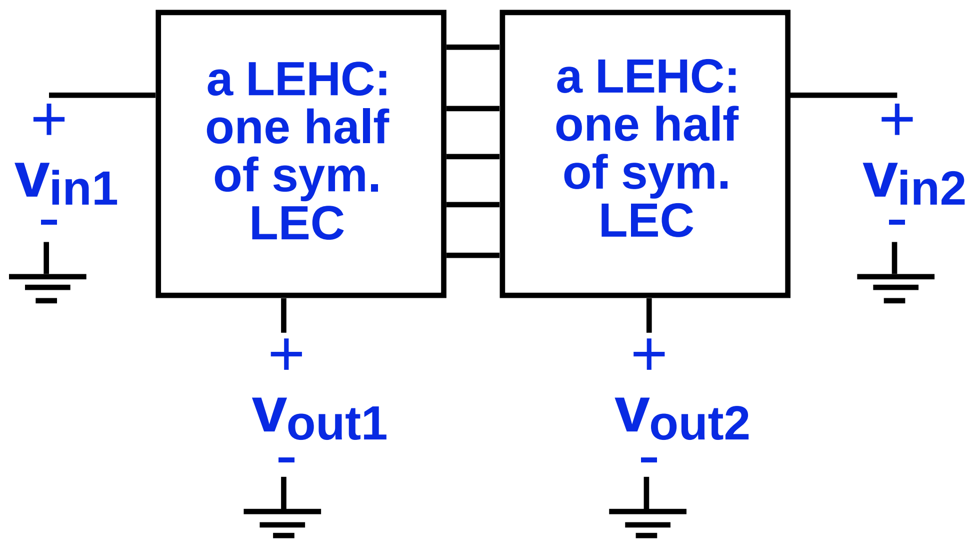
We will apply v_{id} to the circuit and get v_{od} (= $A_{vd}v_{id}$), and then apply v_{ic} to the circuit to get v_{oc} (= $A_{vc}v_{ic}$). Then we will reconstruct our outputs:

$$v_{out1} = v_{oc} + v_{od}/2 = A_{vc}v_{ic} + A_{vd}v_{id}/2$$
$$v_{out2} = v_{oc} - v_{od}/2 = A_{vc}v_{ic} - A_{vd}v_{id}/2$$

Differential Amplifier Analysis -

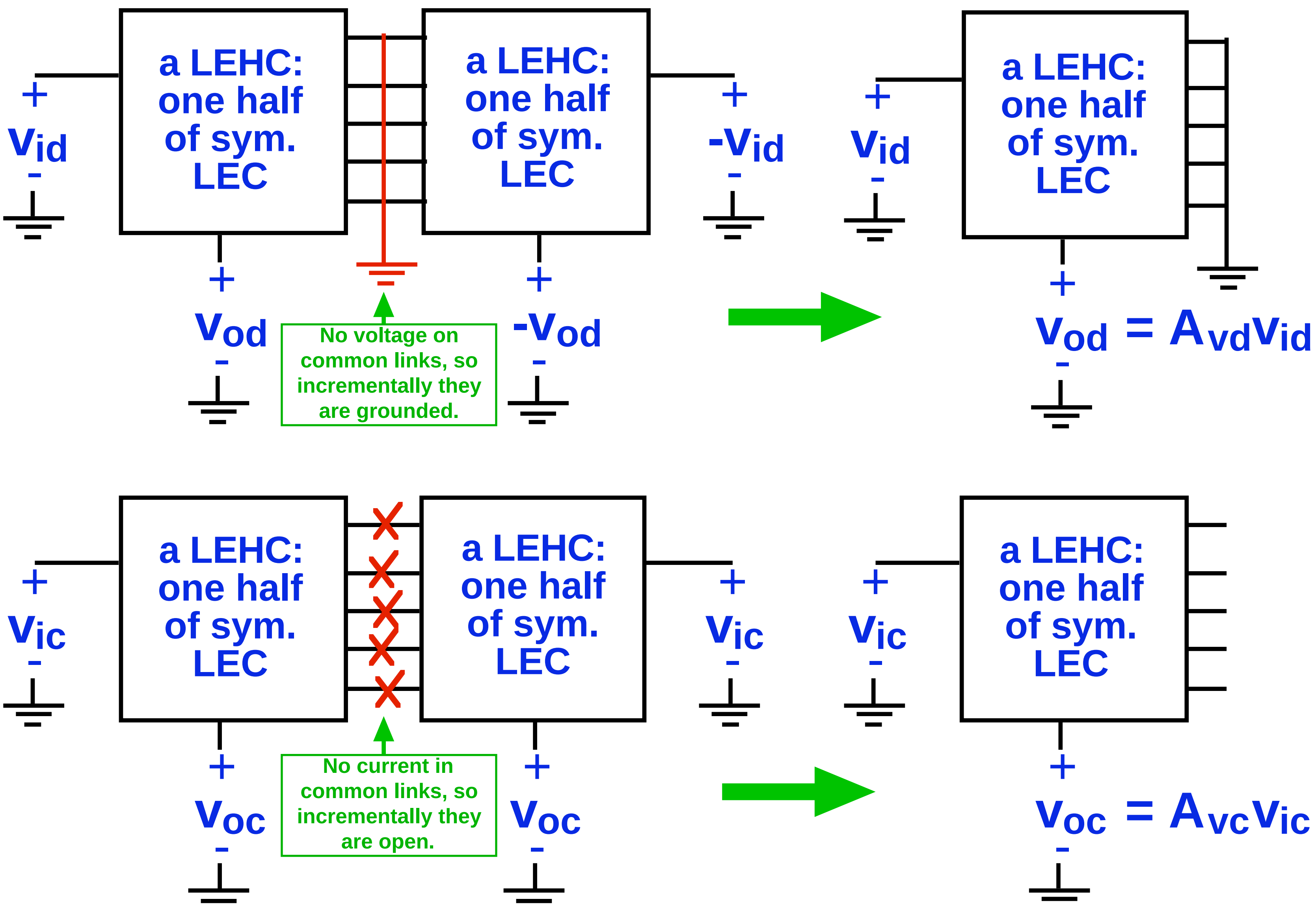
incremental analysis exploiting symmetry and superposition





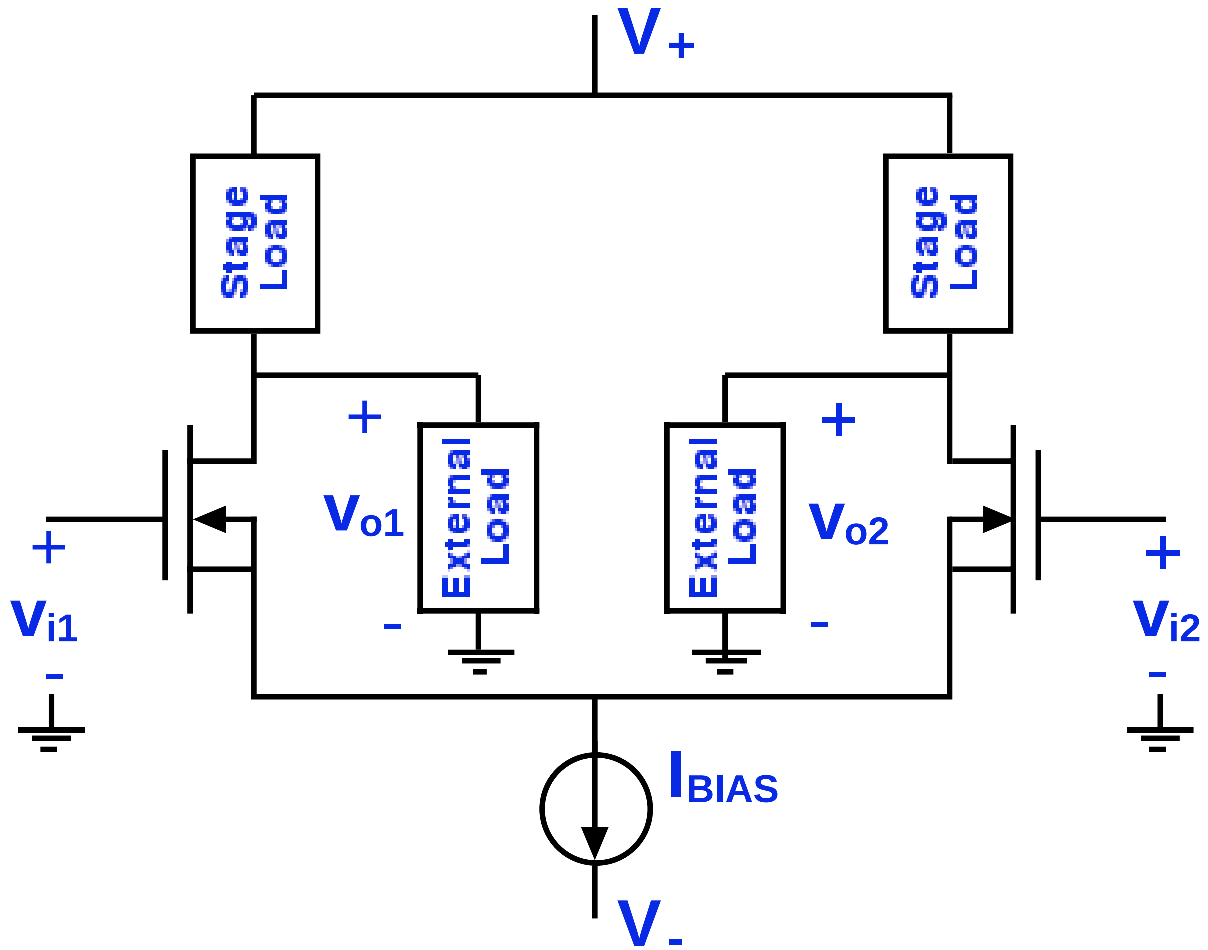
Differential Amplifier Analysis -

incremental analysis exploiting symmetry and superposition



Differential Amplifier Analysis - example of LEC analysis

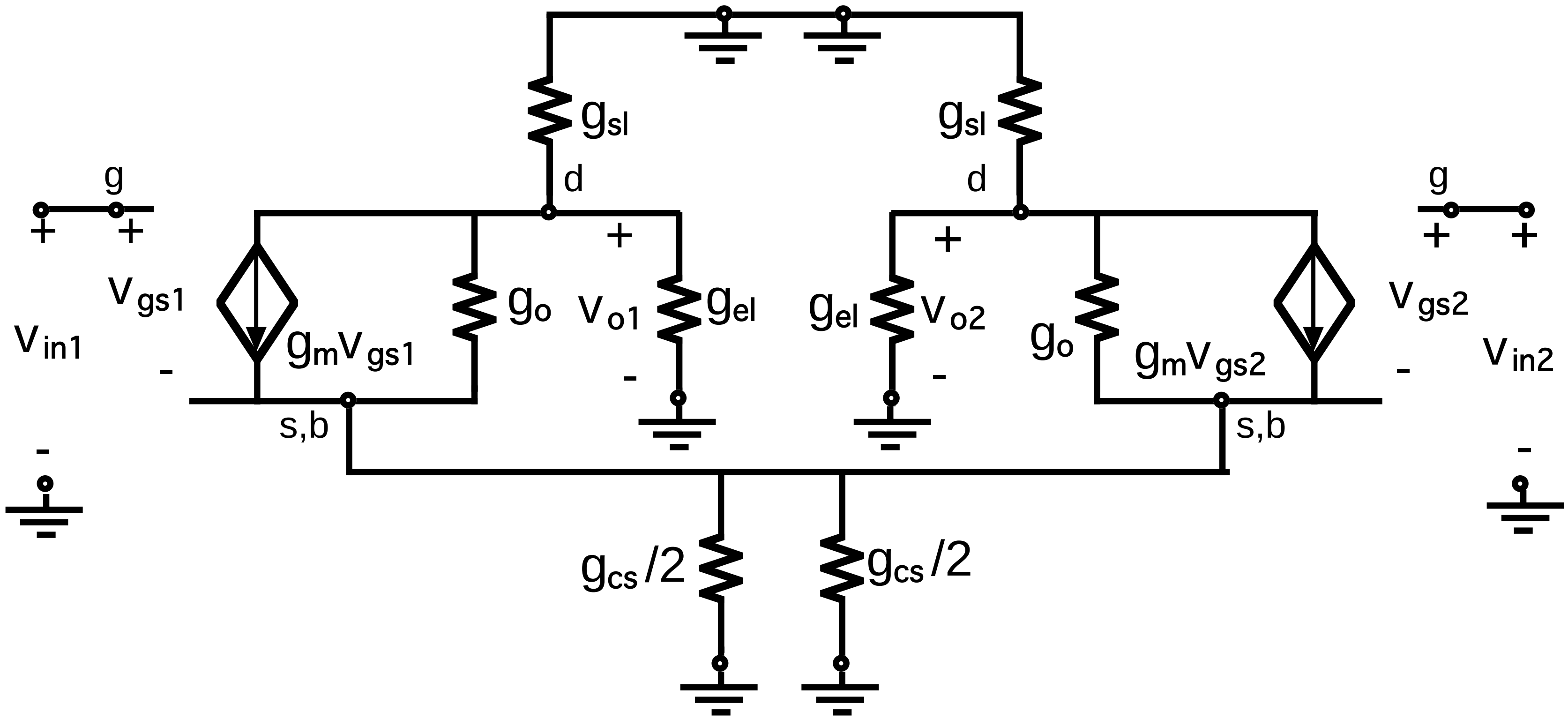
Consider a source-coupled pair:



We begin by drawing the LEC for this differential amplifier....

Differential Amplifier Analysis - example, cont.

The LEC for our amplifier:



We decompose our inputs into common- and difference-mode inputs:

$$v_{id} \equiv v_{in1} - v_{in2}$$

$$v_{ic} \equiv \frac{v_{in1} + v_{in2}}{2}$$

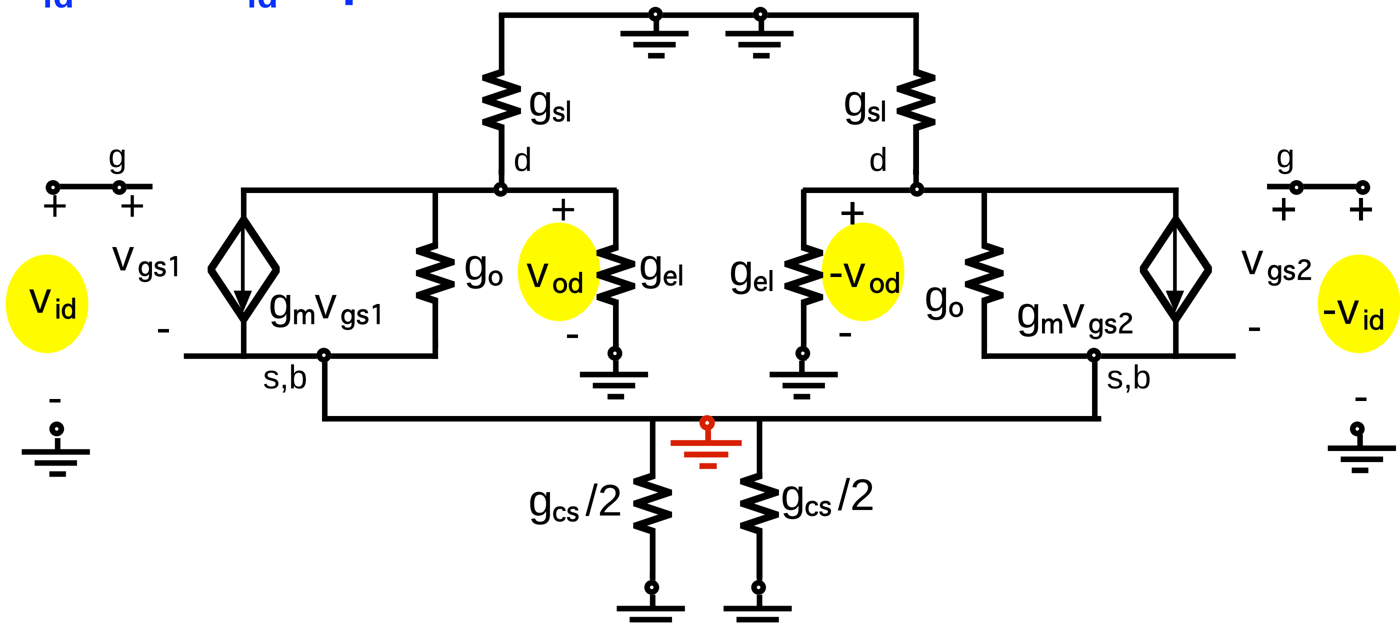
Also:

$$v_{od} \equiv v_{out1} - v_{out2}$$

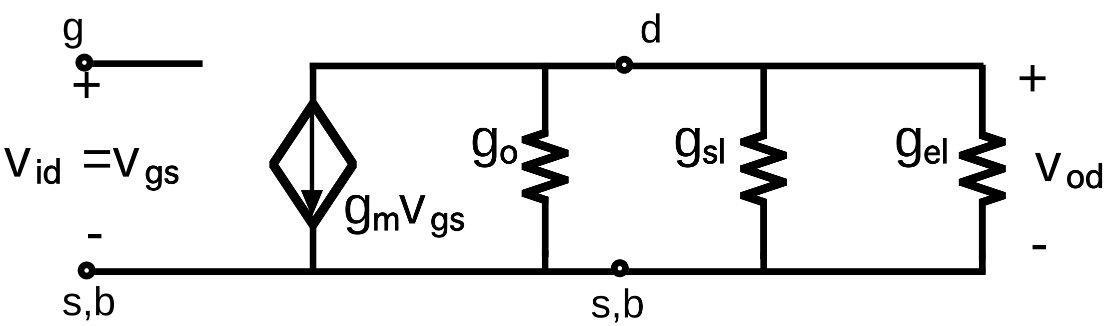
$$v_{oc} \equiv \frac{v_{out1} + v_{out2}}{2}$$

Differential Amplifier Analysis - example, cont.

With v_{id} and $-v_{id}$ inputs:



This LEC simplifies to:



From which:

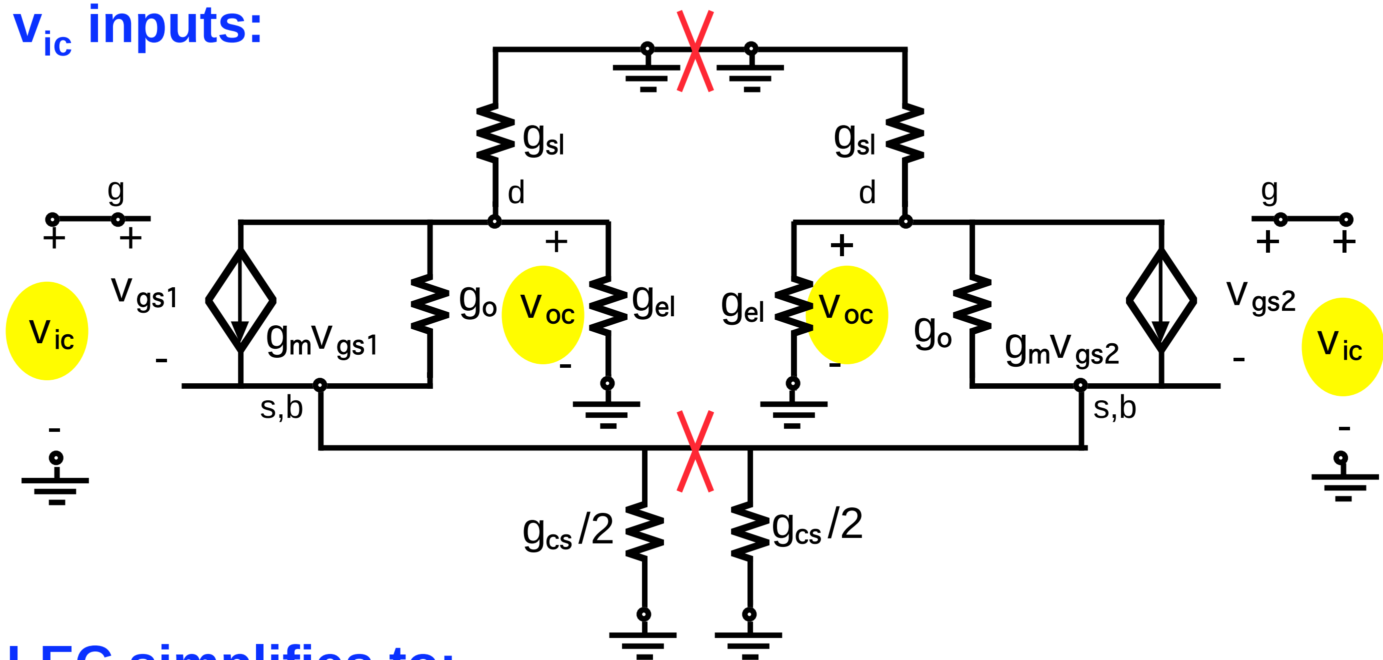
$$v_{od} = \frac{-g_m v_{id}}{(g_o + g_{sl} + g_{el})}$$

$$A_{vd} = \frac{-g_m}{(g_o + g_{sl} + g_{el})}$$

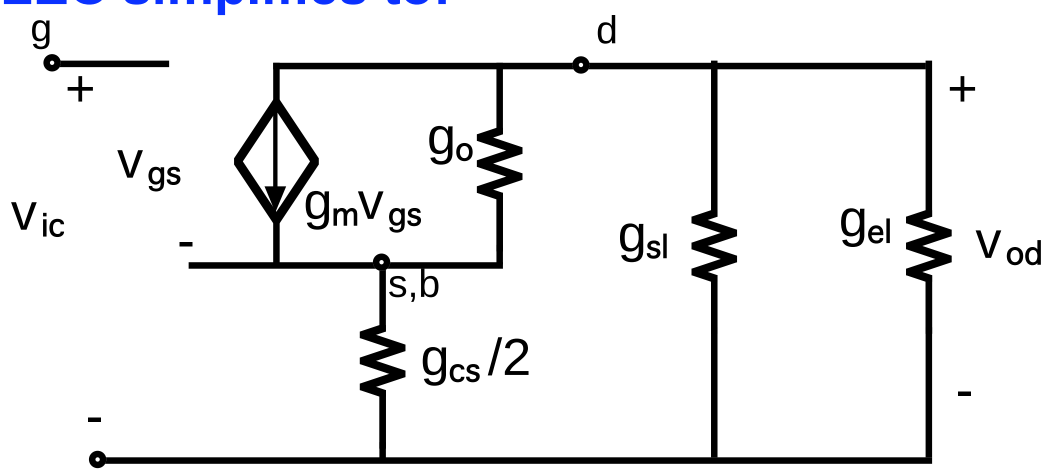
Note: We want A_{vd} to be very large.

Differential Amplifier Analysis - example, cont.

With v_{ic} inputs:



This LEC simplifies to:



From which:

$$v_{oc} \approx \frac{-g_{cs} v_{ic}}{2(g_{sl} + g_{el})}$$

$$A_{vc} \approx \frac{-g_{cs}}{2(g_{sl} + g_{el})}$$

Note: We want A_{vc} to be very small.

Differential Amplifier Analysis - example, cont.

Knowing A_{vd} and A_{vc}, we can construct v_{o1} and v_{o2} :

$$v_{o1} = v_{oc} + \frac{v_{od}}{2} = A_{vc} v_{ic} + \frac{A_{vd} v_{id}}{2}$$

$$= -\frac{g_{cs}}{2(g_{sl} + g_{el})} v_{ic} - \frac{g_m}{2(g_o + g_{sl} + g_{el})} v_{id}$$

$$= -\frac{g_{cs}}{2(g_{sl} + g_{el})} \frac{(v_{i1} + v_{i2})}{2} - \frac{g_m}{2(g_o + g_{sl} + g_{el})} (v_{i1} - v_{i2})$$

$$v_{o2} = v_{oc} - \frac{v_{od}}{2} = A_{vc} v_{ic} - \frac{A_{vd} v_{id}}{2}$$

$$= -\frac{g_{cs}}{2(g_{sl} + g_{el})} v_{ic} + \frac{g_m}{2(g_o + g_{sl} + g_{el})} v_{id}$$

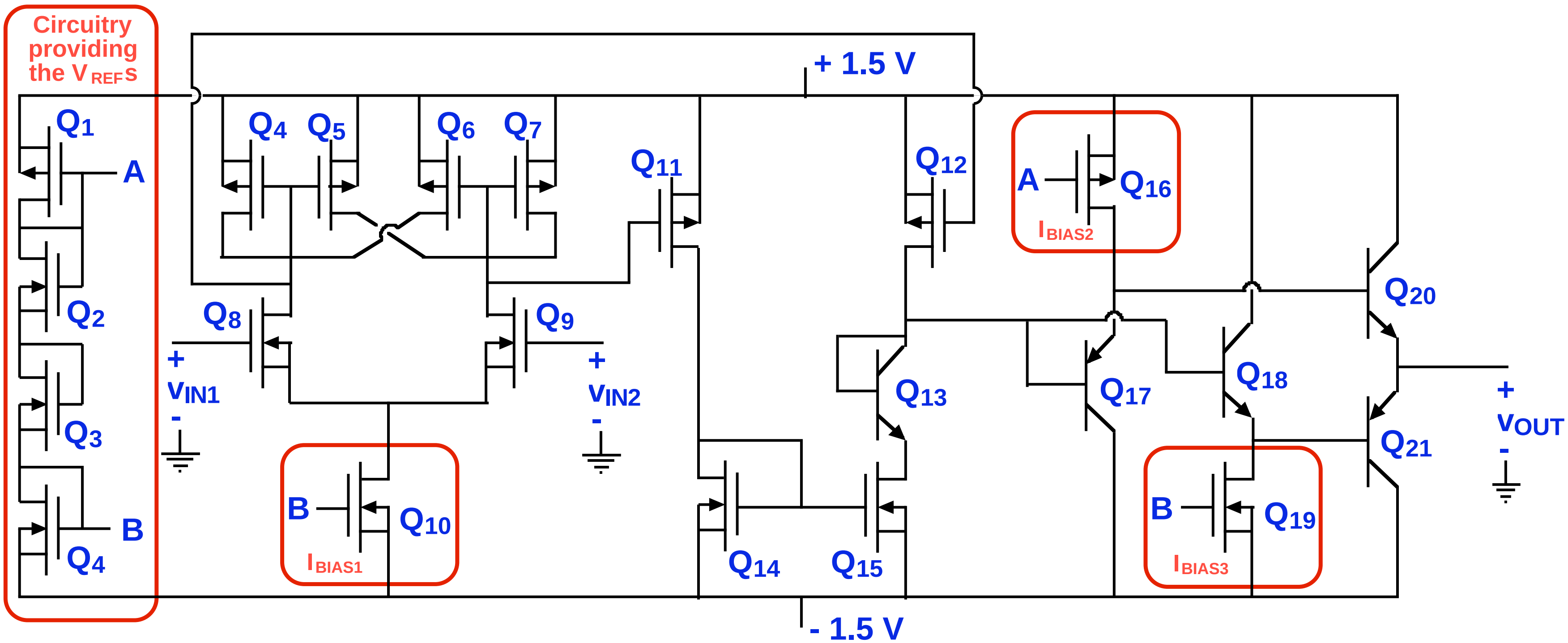
$$= -\frac{g_{cs}}{2(g_{sl} + g_{el})} \frac{(v_{i1} + v_{i2})}{2} + \frac{g_m}{2(g_o + g_{sl} + g_{el})} (v_{i1} - v_{i2})$$

Remember: In a good Diff Amp $|A_{vd}|$ is very large, and $|A_{vc}|$ is very small.

Looking at a complicated circuit:

Lesson I - Find the biasing circuitry and represent it symbolically

Consider the following example:



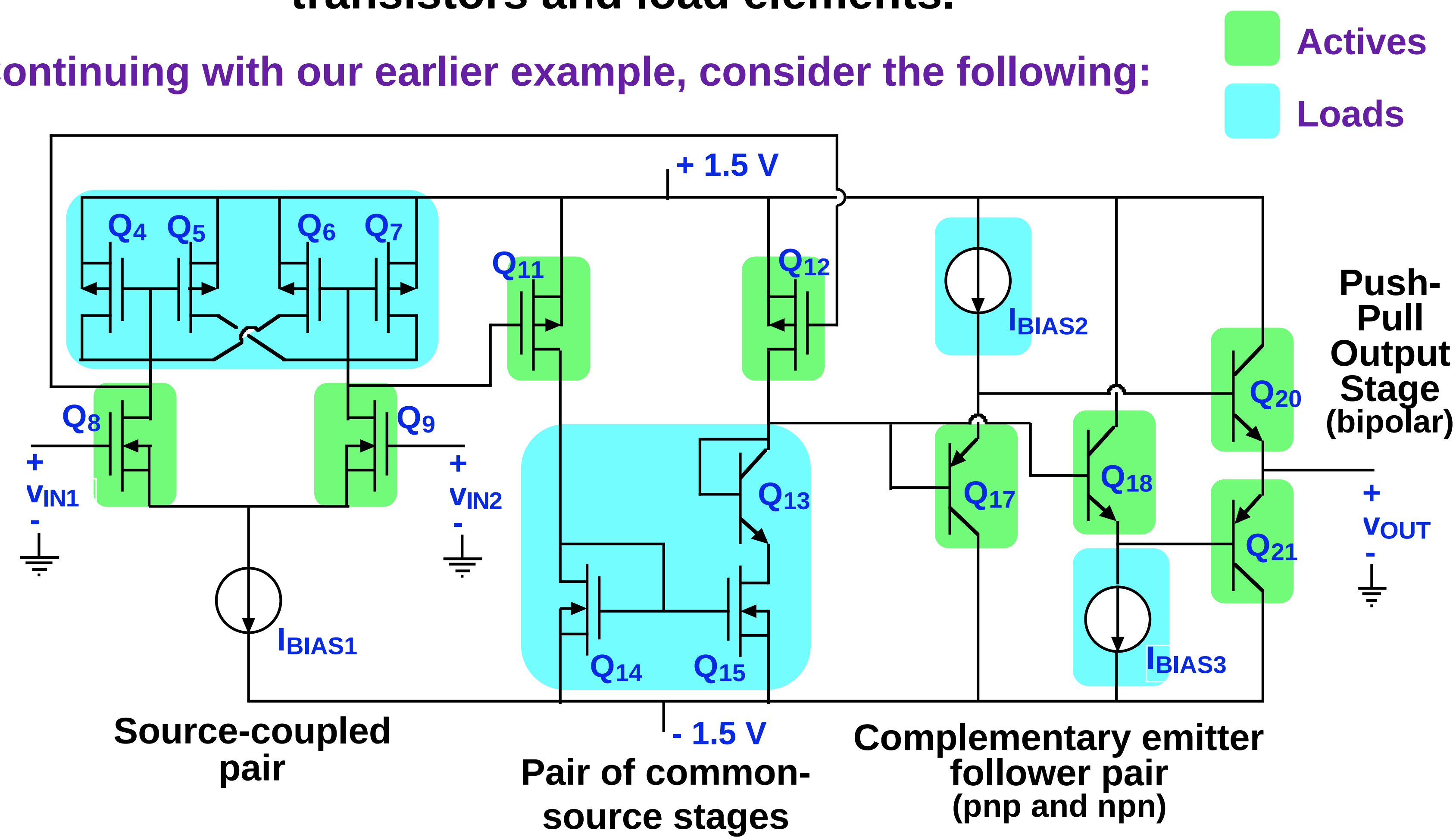
7 of the 21 transistors are used for biasing the other 14 transistors.

If we get the biasing transistors out of the picture for awhile, the circuit looks simpler. (next foil)

Looking at a complicated circuit:

Lesson II - Identify the individual stages and their active transistors and load elements.

Continuing with our earlier example, consider the following:

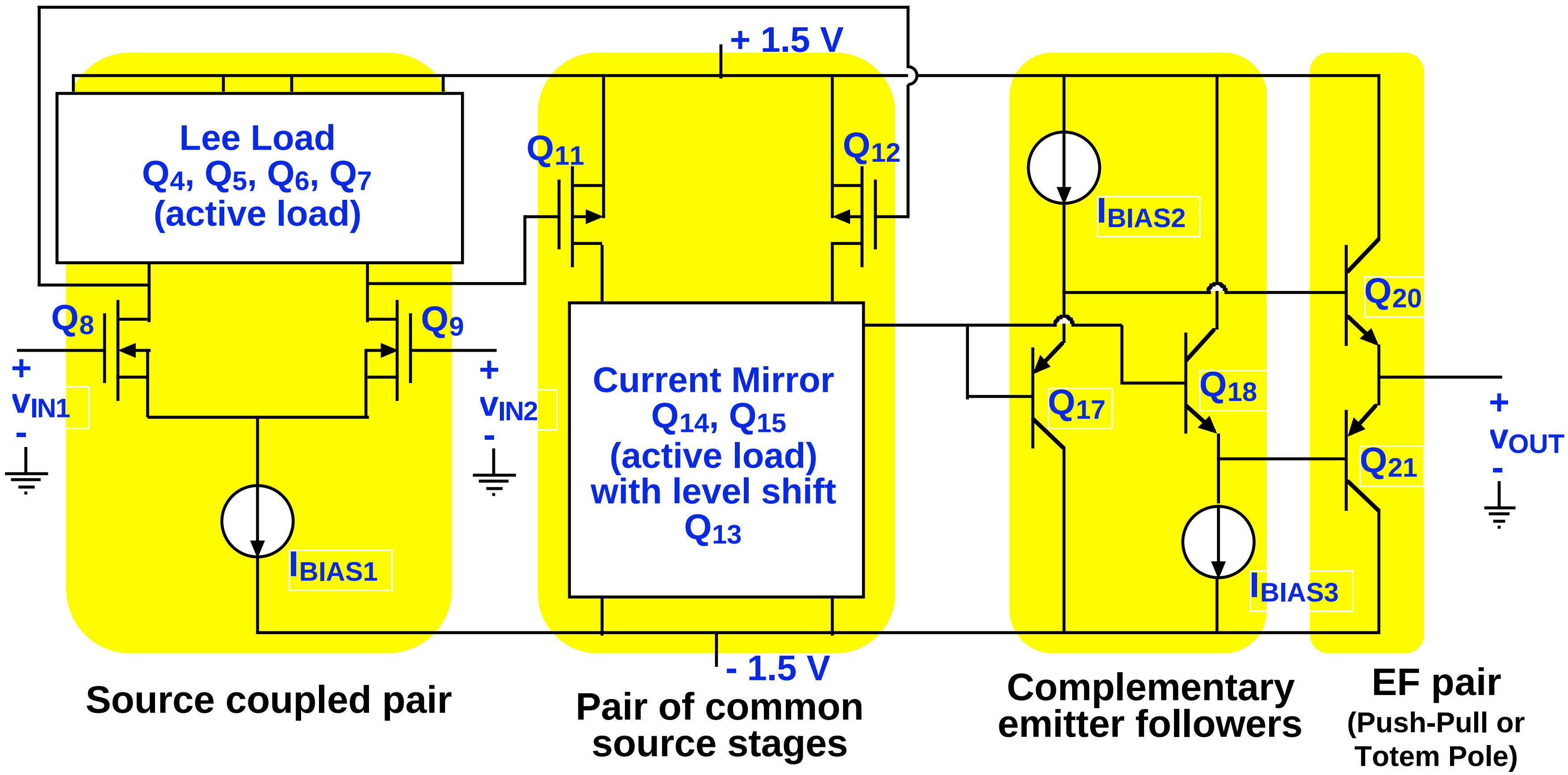


Note: We can almost make sense of all of the stages, but we still need to study active loads and output stages to fully understand them.

Looking at a complicated circuit:

Lesson III - Use half-circuit techinques to convert the differential stages to familiar single transistor stages.

Continuing with the same example:

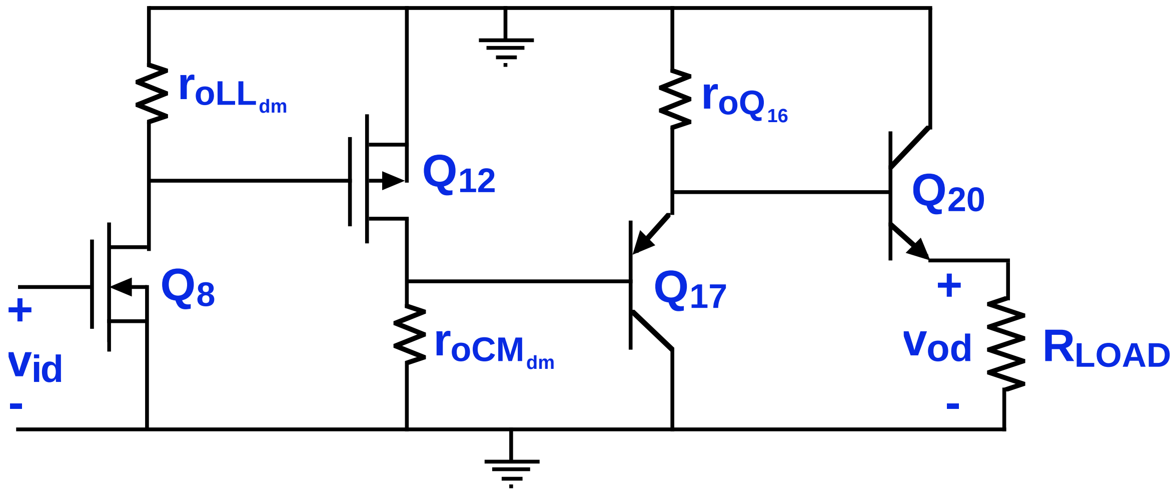


There are two symmetrical differential gain stages, followed by two complementary output stages (next foil)

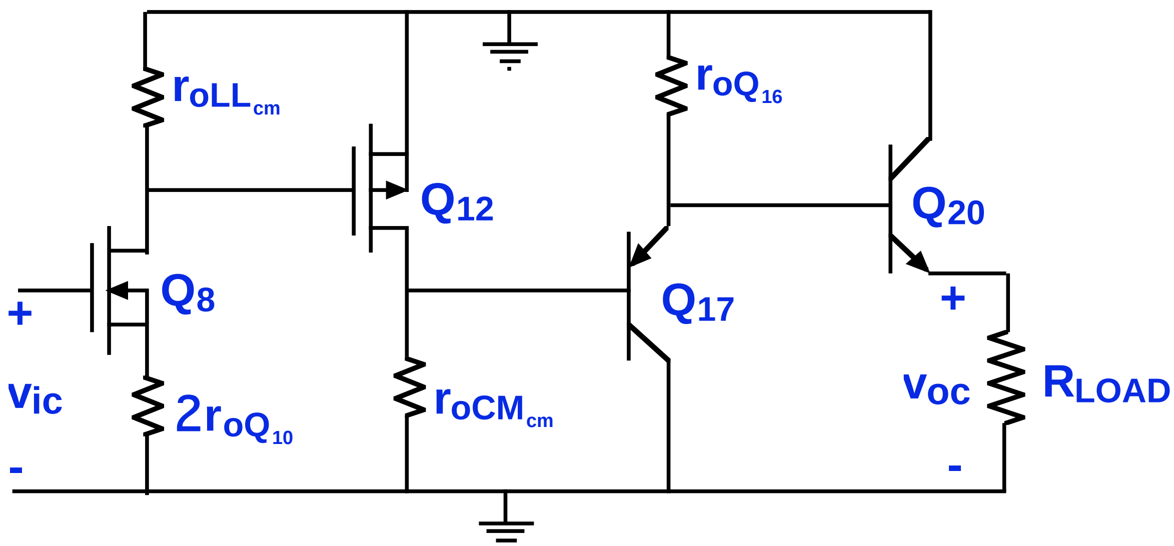
Looking at a complicated circuit:

Lesson III, cont. - Draw the difference and common mode half circuits.

Difference mode half circuit:



Common mode half circuit:



Voila!! We have reduced the transistor count from 21 to 4, and we see that our complex amplifier is just a cascade of 4 single-transistor stages.

Lecture 19 - Differential Amplifier Stages - Summary

- **Differential Amplifier Stages - Large signal behavior**

  General features: two transistors **(a source-coupled, or emitter-coupled, pair)**
  highly symmetrical
  two inputs, two outputs **(Note: one input can be zero)**
  biased by single current source

  Large signal transfer characteristic: only depends on $v_{IN1} - v_{IN2}$

- **Difference- and common-mode signals**

  Difference-mode: $v_{ID} = v_{IN1} - v_{IN2}$
  Common-mode: $v_{IC} = (v_{IN1} + v_{IN2})/2$
  Reconstruction: $v_{IN1} = v_{ID} + v_{IC}/2$, $v_{IN2} = v_{ID} - v_{IC}/2$

- **Half-circuit incremental analysis techniques**

  Exploiting symmetry and superposition
  Difference-mode lin. equiv. half-circuit: links are grounded
  Common-mode lin. equiv. half circuit: links are cut, open circuited
  Approach: 1. identify common- and difference-mode half circuits
  2. calculate common- and difference-mode signals
  3. analyze difference-mode half-circuit
  4. analyze common-mode half-circuit
  5. reconstruct signals

  (each half-circuit is one of our known building-blocks)

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