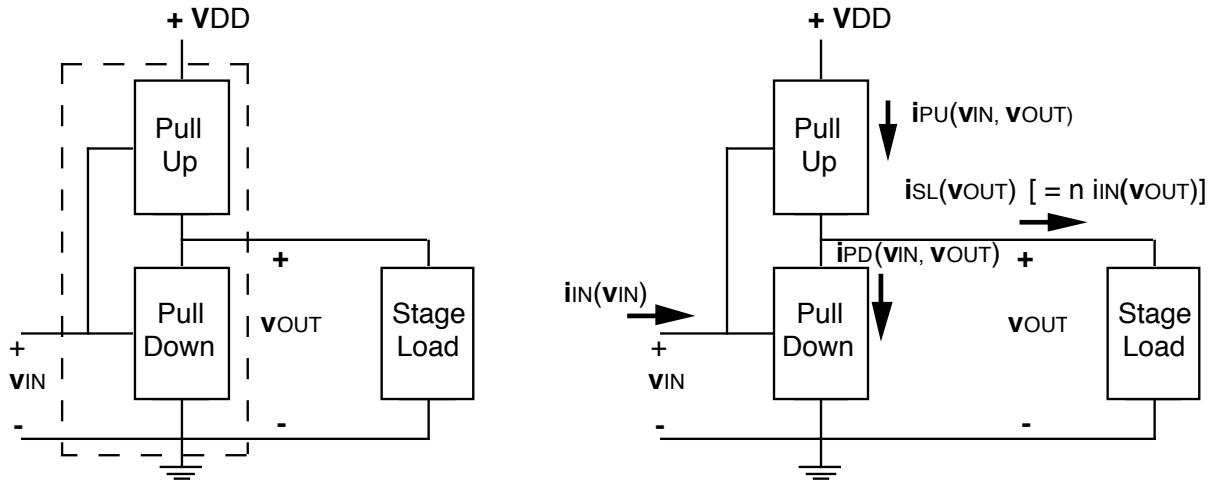
6.012 - Microelectronic Devices and Circuits – Fall 2009

Inverter Analysis and Design

The inverter stage is a basic building block for digital logic circuits and memory cells. A generic inverter stage is illustrated below on the left. It consists of two devices, a pull-up device, which is typically either a bipolar junction transistor or an enhancement mode field effect transistor, and a pull-down device, which might be another transistor, or a resistor, current source, diode, etc. The stage load which is shown in the figure represents the input resistance of the following stage, which is typically a stage (or n stages) just like the original stage.



(a) A generic inverter stage (b) The static currents to calculate $v_{OUT}(v_{IN})$

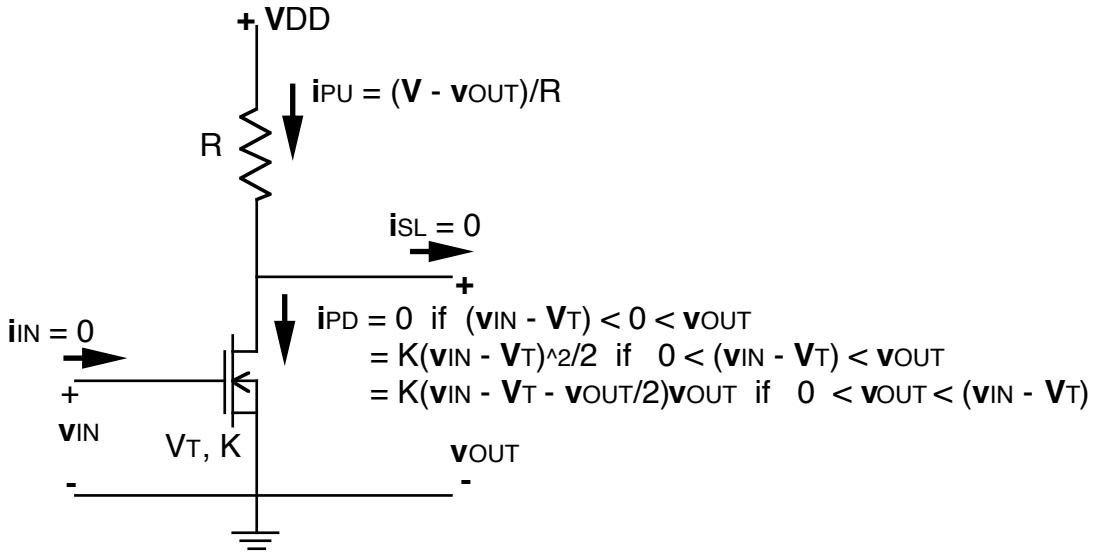
An important piece of information about an inverter stage is its static transfer characteristic, $v_{OUT}(v_{IN})$. To calculate this characteristic we sum the currents into the output node of the inverter, as is illustrated above on the right. With all of these currents written as functions of v_{IN} and v_{OUT}, this sum yields the desired relationship:

$$i_{PU}(v_{IN}, v_{OUT}) = i_{PD}(v_{IN}, v_{OUT}) + i_{SL}(v_{OUT})$$

As an example, consider the MOSFET inverter circuit shown at the top of the next page with an n-channel MOSFET pull-down and a resistor pull-up. The MOSFET is characterized by its K-value and by its threshold voltage, V_T (we will assume for simplicity that α is 1). To analyze this circuit we not first that with a MOSFET pull-down, the static input current is zero and if the stage output is connected to the input of a similar stage, the static stage load current will also be zero, and the equation above is simply $i_{PU} = i_{PD}$. With a resistor pull-up, the pull-up current, i_{PU}, is $(V_{DD} - v_{OUT})/R$ and the pull-down current, i_{PD}, is the MOSFET drain current. This current depends on the gate-to-source voltage, v_{GS}, which is the same as v_{IN}, and the drain-to-source voltage, v_{DS}, which is the same as v_{OUT}. With v_{IN} less than V_T, the pull-down current is zero and v_{OUT} is V_{DD}. As v_{IN} increases past V_T, v_{OUT} will initially be larger than

(v_{IN} - V_T), and the device will be in saturation so that i_{PD} will be $K(v_{IN} - V_T)^2/2$. v_{OUT} is found by setting i_{PD} equal to i_{PU}:

$$i_{PU} = i_{PD}$$



A MOSFET inverter with an n-channel MOSFET pull-down and resistor pull-up.

Substituting yields

$$(V_{DD} - v_{OUT})/R = K(v_{IN} - V_T)^2/2$$

which we solve for v_{OUT}

$$v_{OUT} = V_{DD} - RK(v_{IN} - V_T)^2/2$$

Clearly v_{OUT} decreases as v_{IN} increases. When v_{OUT} reaches v_{IN} - V_T, the pull-down goes from saturation to the linear region and i_{PD} changes to $K(v_{IN} - V_T - v_{OUT}/2)v_{OUT}$, and the desired relationship is found by solving the quadratic

$$(V_{DD} - v_{OUT})/R = K(v_{IN} - V_T - v_{OUT}/2)v_{OUT}$$

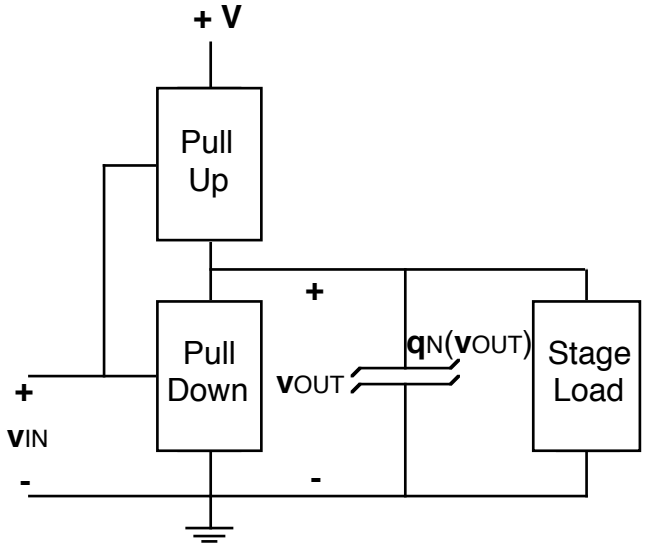
The resulting transfer characteristic is plotted in the course text in Figure 15.8. Curves for other pull-up devices are also shown in this section of the text.

We can identify six features of a given inverter design which we can use to evaluate it and compare it to other designs. They are:

1. The logic levels, V_{HI}, and V_{LO}
2. The noise margins
3. The switching times, $\tau_{HI \rightarrow LO}$, and $\tau_{LO \rightarrow HI}$
4. The power dissipation
5. The fan-out and fan-in sensitivities
6. The manufacturability

The **logic levels** are found by insisting that V_{HI} and V_{LO} are such that V_{HI} applied to the input of an inverter results in an output of V_{LO}, and that V_{LO} applied to the input of an inverter results in an output of V_{HI}. Mathematically, if the transfer characteristic is $v_{OUT} = f(v_{IN})$, we must find the solutions to the equation $v_{OUT} = f(f(v_{OUT}))$. For useful inverter stages there will be three solutions to this equation, but only the largest and smallest values are valid; the middle solution is unstable and will not be realized in practice. V_{HI} and V_{LO} are often most easily found with the aid of the graphical technique shown in Figure 15.5 of the course text.

To determine the **switching times** we must first recognize that the reason an inverter output does not instantaneously change in response to an change of its input is because there is charge stored on the output node (on the gate of the load stage, for example, if we are discussing inverters with MOSFET pull-downs as in our earlier example). This is illustrated below:



The generic inverter stage with the non-linear charge store shown explicitly.

When the input is switched from V_{HI} to V_{LO}, the pull down device typically turns off (so $i_{PD} = 0$), and the output switches from V_{LO} to V_{HI}. When this happens the output node must be charged up, and this charge is supplied by the pull-up device. This was illustrated on the left in the next figure. The charging current, i_{CH}, which is dq_N/dt, is the difference between i_{PU} and i_{SL} (assuming as is usually the case that $i_{PD} = 0$):

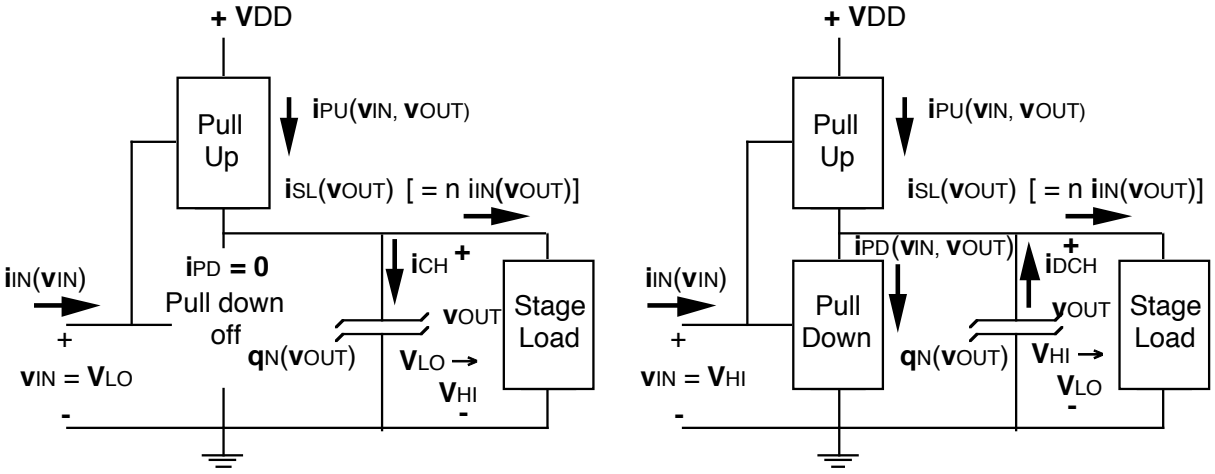
$$i_{CH} \approx i_{PU} - i_{SL} = dq_N/dt$$

The larger this current, the faster the charge store changes, and the faster the output switches. (Note that the corresponding statements can be made about the discharging cycle shown on the right in the figure.)

In general the charge stored on the output node, q_N, will be a non-linear function of v_{OUT}, and it will not be possible to calculate $v_{OUT}(t)$ and determine the switching time analytically. There are two cases in which we can calculate the switching time,

however, and to the extent that we can approximate a given situation as one or the other of these to cases, we can estimate the switching time analytically.

The first special case is when the charging (or discharging) current is constant. We can calculate the change in the amount of stored charge when v_{OUT} changes from V_{LO} to V_{HI}, and knowing this the charging time is simply this charge divided by the



(a) Finding $\tau_{LO\to HI}$ (charging cylce)
v_{IN}: $V_{HI}\to V_{LO}$; v_{OUT}: $V_{LO}\to V_{HI}$
$i_{CH} = i_{PU} - i_{PD} - i_{SL}$

(b) Finding $\tau_{HI\to LO}$ (discharge cycle)
v_{IN}: $V_{LO}\to V_{HI}$; v_{OUT}: $V_{HI}\to V_{LO}$;
$i_{DCH} = i_{PD} - i_{PU} + i_{SL}$

charging current, which we have approximated as being constant, I_{CH} (we can say the same about the discharge cycle):

$$\tau_{LO\to HI} \approx \Delta q_N / I_{CH}, \quad \text{and} \quad \tau_{HI\to LO} \approx -\Delta q_N / I_{DCH}$$

[Note: frequently designers do not require that the node be completely charged, but say the node has switched when 90% of the store has been built up (in which case, of course, Δq_N is replaced by $0.9\,\Delta q_N$].

The second special case is if the charge store can be modeled as a linear capacitor, C_L (i.e., $q_N \approx C_L v_{OUT}$). Then we can write

$$dv_{OUT}/dt = i_{CH}(v_{OUT})/C_L$$

to get a differential equation for $v_{OUT}(t)$. We should be able to solve this equation numerically, if we can not do so analytically.

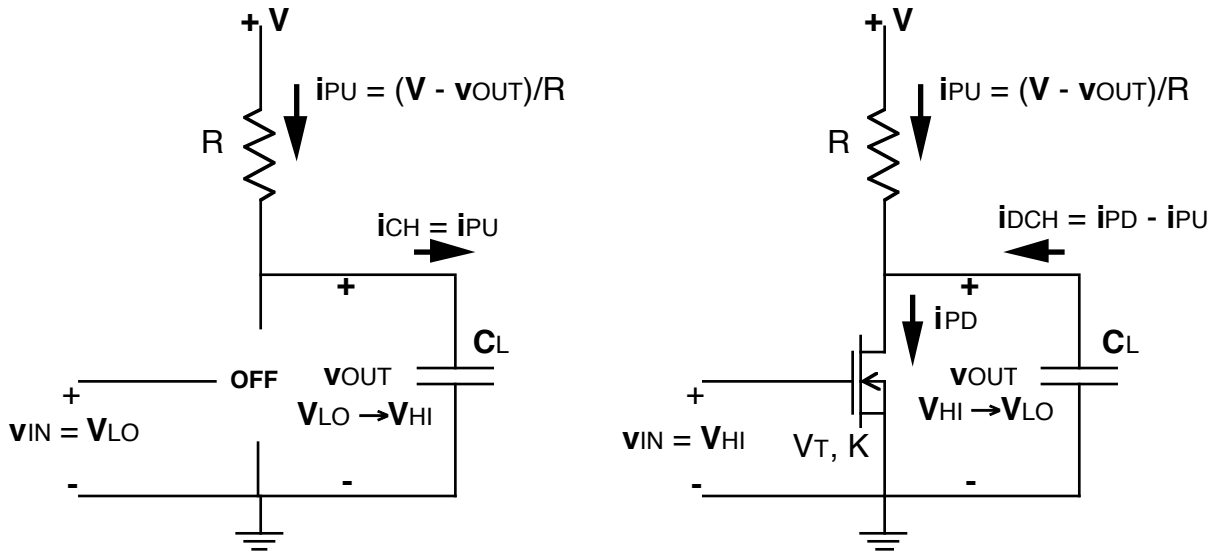
If the charge store can be modeled as a linear capacitor and the charging and dischargind currents can be modeled as constant, then

$$\tau_{LO\to HI} \approx C_L(V_{HI} - V_{LO})/I_{CH}, \quad \text{and} \quad \tau_{HI\to LO} \approx C_L(V_{HI} - V_{LO})/I_{DCH}$$

We have already included the transient when the input is switched from V_{LO} to V_{HI} in our discussion, but just to make sure this is clear, in this part of the cycle, the pull down device turns on and the output switches from V_{HI} to V_{LO}. The most important difference is that the charge store now discharges and does so through the pull-down device. The pull-down device must conduct this discharge current and the current flowing through the pull-up device (less that into the stage load). In this case, a large pull-up device current is not desirable because it makes this switching time long, whereas a large pull-up current makes the other switching time short.

In practice one usually wants to minimize the sum of these two switching times which means that we in general want to design the circuit to have equal magnitude charging and discharging currents, if possible.

An example to the switching transient situation in the MOSFET inverter with a resistive pull-up that we illustrated earlier is shown in the figures below. The gate capacitance of the loading stage(s) has been modeled as a linear capacitor. The charging of the store clearly occurs with an RC time constant exponential; the discharging transient is more complex (and typically is much the shorter of the two).



(a) Finding $\tau_{LO\to HI}$ (charging cylce)
v_{IN}: $V_{HI}\to V_{LO}$; v_{OUT}: $V_{LO}\to V_{HI}$
$i_{CH} = i_{PU}$

(b) Finding $\tau_{HI\to LO}$ (discharge cycle)
v_{IN}: $V_{LO}\to V_{HI}$; v_{OUT}: $V_{HI}\to V_{LO}$;
$i_{DCH} = i_{PD} - i_{PU}$

The **power dissipation** consists of two components. One is the static power; the other is the dynamic, or switching, power. Then the ouput is high, the static power dissipated is $V_{DD}I_{PU}$(output high); when the output is low, the static power dissipated is $V_{DD}I_{PU}$(output low). To get one number to work with we commonly say an average inverter will have its output high half the time, on average, and low the other half. Thus the average static power dissipation is ($V_{DD}I_{PU}$(output high) + $V_{DD}I_{PU}$(output low))/2.

The dynamic power dissipation is due the fact that each low-high-low cycle the output node is charged to roughly V_{DD}, and then discharged to roughly zero volts. If we can approximate the node charge store with a linear capacitor, C_L, the energy dissipated in charging it to V_{DD} is $C_L V_{DD}^2/2$, and the amount of energy stored on the node is also $C_L V_{DD}^2/2$. This later amount of energy is dissipated when the node is discharged so in one cycle the total energy dissipated is $C_L V_{DD}^2$. If the gate is operating at a frequency of f, the average dynamic power dissipation is f times this or f $C_L V_{DD}^2$.

You can refer to the course text for discussions of **noise margins**, **fan in and fan out**, and **manufacturability**.

6.012 Microelectronic Devices and Circuits
Fall 2009