*YOUR NAME*_____

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology

6.012 Microelectronic Devices and Circuits

Final Exam

Closed Book: Formula sheet provided; 3 sheets of notes permitted

Notes:

1. Unless otherwise indicated, you should assume room temperature and that kT/q is 0.025 V. You should also approximate [(kT/q) ln 10] as 0.06 V.
2. Closed book; formula sheet provided and three sheets (6 pages) of notes permitted.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded. You are advised to show as much of your work as possible, and to cross out things you think are wrong, rather than erasing them.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
5. Be careful to include the correct units with your answers when appropriate.
6. Be certain that you have all thirteen (13) pages of this exam booklet and the eight (8) page formula sheet, and make certain that you write your name at the top of this page in the space provided.
7. An effort has been made to make the various parts of these problems independent of each other so if you have difficulty with one item go on, and come back later.
8. You may see your graded final exam in Room 13-3058 beginning January 6, 2010.

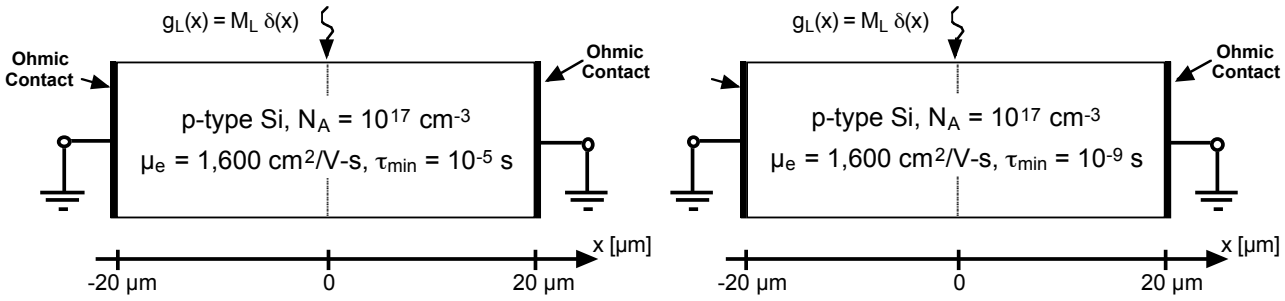
6.012 Staff Use Only	**PROBLEM 1**	_____	(out of a possible 25)
	PROBLEM 2	_____	(out of a possible 25)
	PROBLEM 3	_____	(out of a possible 25)
	PROBLEM 4	_____	(out of a possible 25)
	TOTAL		

Problem 1 - (25 points)

Three short problems:

a) [8 pts] Consider the two bars of p-type Si, N_A, = 10^{17} cm^{-3} illustrated below. They are 40 μm long with ohmic contacts on each end, and are identical except that in one the minority carrier lifetime, τ_{min}, is 10^{-5} s, and in the other it is 10^{-9} s. The electron mobility, μ_e, is the same, 1,600 cm^2/V-s, in both.

The bars are illuminated with constant radiation generating M_L hole-electron pairs/cm^2-s uniformly across the plane at x = 0, i.e. $g_L(x,t) = M_L\delta(x)$.



i) What is the minority carrier diffusion length, L_{min}, in each sample?

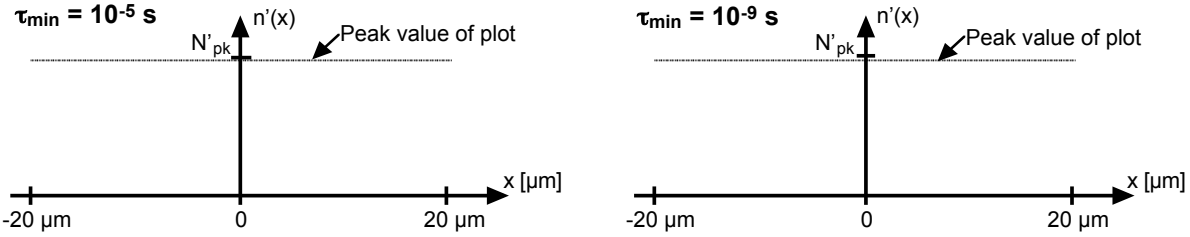
Longer lifetime sample (τ_{min} = 10^{-5} s):

L_{min} = _____ μm

Shorter lifetime sample (τ_{min} = 10^{-9} s):

L_{min} = _____ μm

ii) On the axes provide, sketch the excess minority carrier populations, n′(x), in each sample for -20 μm ≤ x ≤ 20 μm. Indicate in the spaces provided the approximate functional shape (e.g. sin x, e^x, x^2, etc.) of the curve, its initial slope at x = 0^+, and its values at x = ± 20 μm.



Functional shape:

n′(±20 μm) =

$dn'/dx|_{x=0+}$ =

Functional shape:

n′(±20 μm) =

$dn'/dx|_{x=0+}$ =

Problem 1a continues on the next page

Problem 1a continued

iii) In which sample is the value of N'_{pk} larger? Explain your answer.

_____ $\tau_{min} = 10^{-5}$ s sample, _____ $\tau_{min} = 10^{-9}$ s sample, _____ They are similar because

b) [8 pts] This question concerns the design and operation of CMOS inverters in the sub-threshold region.

i) In the space to the right draw the circuit schematic of a standard CMOS inverter indicating the type of each transistor (n-MOS or p-MOS), and labeling the sources, drains, and gates (S,D,G), and the input, output, and supply voltages (v_{IN}, v_{OUT}, and V_{DD}).

ii) Designing CMOS to operate in the sub-threshold region makes it possible to make very low power, albeit slow, digital integrated circuits. Which of the options below for designing CMOS to operate in the sub-threshold region is the most effective in lowering the power dissipation per gate?

_____ By designing transistors with threshold voltages of larger magnitude, $|V_T|$ than are conventionally used along with conventional V_{DD} values.

_____ By using smaller supply voltages, V_{DD}, than are conventionally used.

_____ By using transistors with much longer gate lengths than conventionally used so the drain currents are very small.

Explain your answer:

iii) Write expressions for the drain currents of the transistors in the schematic you drew in Part b) i) in terms of v_{IN}, v_{OUT}, and V_{DD} assuming they are operating in the sub-threshold region: $i_D = I_{ST} \exp(v_{GS}/V_t) [1 - \exp(-v_{DS}/V_t)]$ where $V_t \equiv kT/q$.

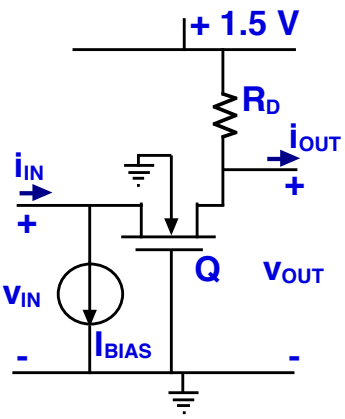
iv) Below write the equation you would solve to calculate the transfer characteristic of your sub-threshold CMOS inverter.

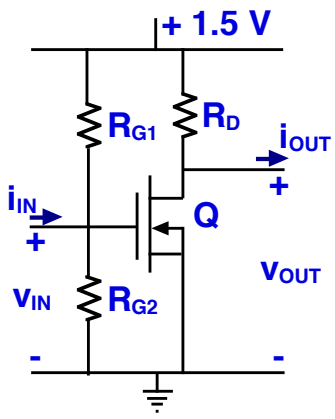
Problem 1 continues on the next page

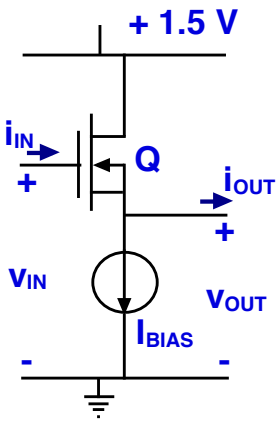
Problem 1 continued

c) [9 pts] A transimpedance amplifier, which is the subject of this question, is an amplifier that generates a small-signal output voltage proportional to the small-signal input current. It is also called a current-to-voltage converter. Typically this circuit has very low input and output resistance to maximize the current-to-voltage conversion.

i) Three single-transistor stages that can be used to build transimpedance amplifiers are illustrated below. Label each of these stages (i.e., common-base, source-follower, etc.) on the line provided below each schematic.

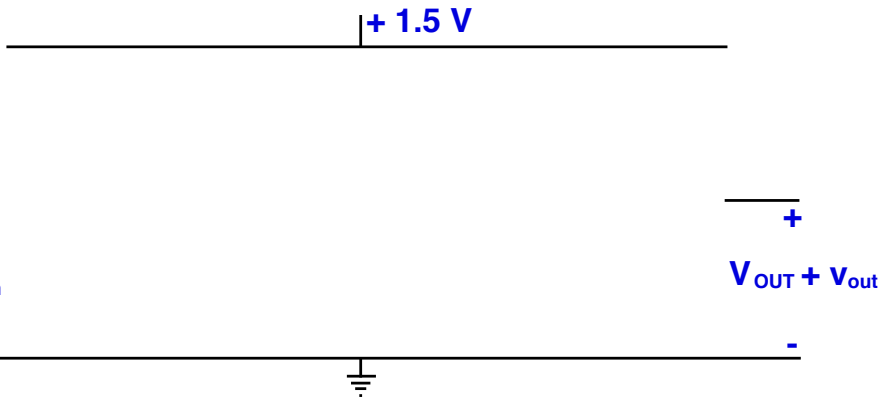






ii) Use a combination of these single-transistor amplifier stages to design a two-stage amplifier with the lowest possible input resistance and the lowest possible output resistance. Indicate your selection of stages, and draw the schematic of your amplifier below.

Stage choices: Stage 1: _____ ; Stage 2: _____



iii) Find expressions for the input and output resistances of your amplifier.

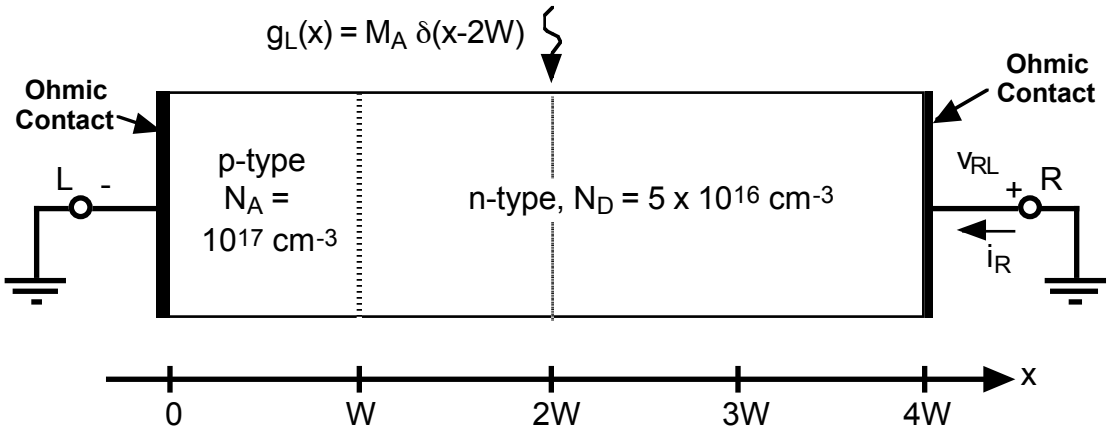
r_{in} = _____ Ω

r_{out} = _____ Ω

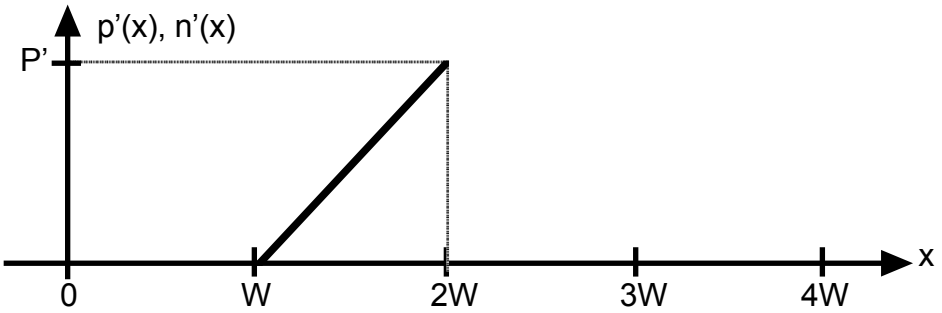
End of Problem 1

Problem 2 (25 points)

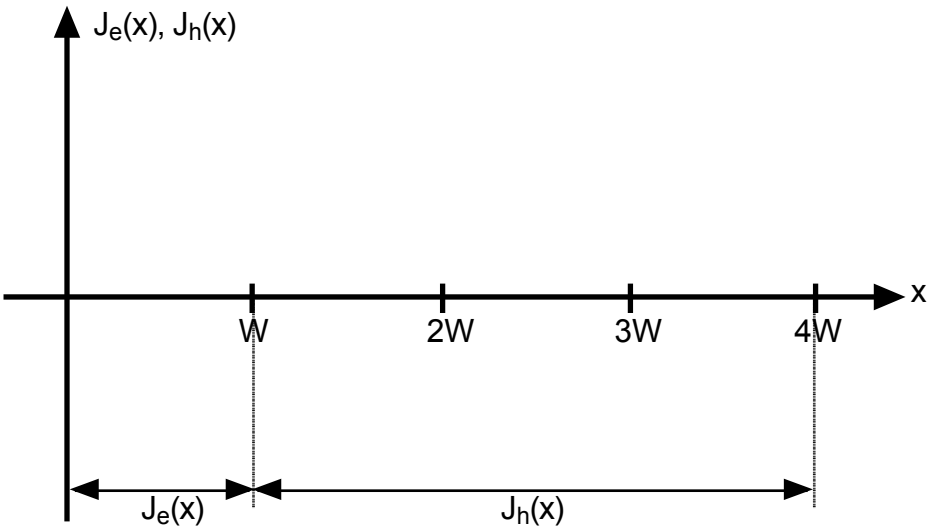
The p-n diode structure below is illuminated with light generating M hole-electron pairs per cm^2-s in the plane at x = 2W, as indicated in the drawing. The intensity of the illumination is sufficiently low that all of the classic flow-problem assumptions hold: low level injection, quasi-neutrality, negligible minority carrier drift, and quasi-static excitation. In this diode the minority carrier lifetime is infinite, the hole mobility is 600 cm^2/V-s, and the electron mobility is 1600 cm^2/V-s.



a) [4 pts] A partial plot of the excess minority carrier concentrations, n'(x) and p'(x) in this sample is shown below. Complete this plot for all x. Ignore the depletion region widths.



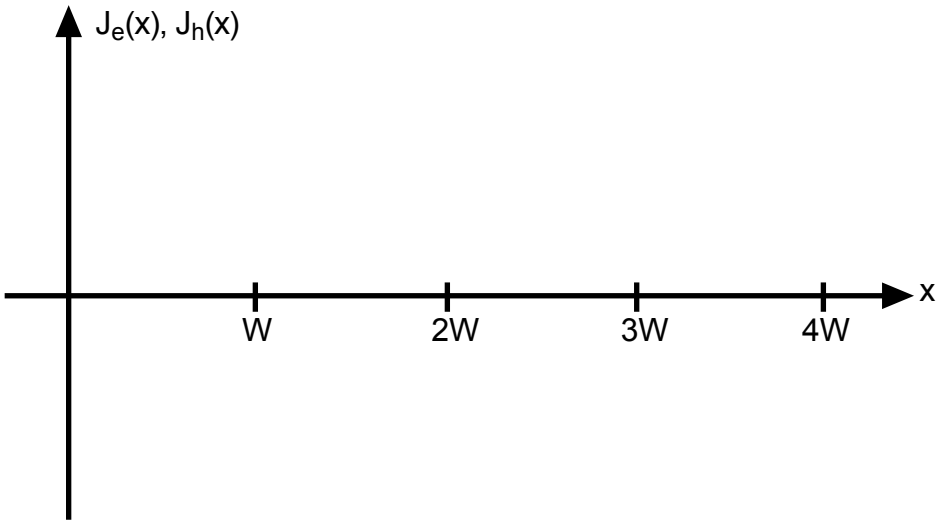
b) [4 pts] On the axes provided, plot the minority carrier current densities throughout the structure, i.e. $J_e(x)$ for $0 \le x \le W$, and $J_h(x)$ for $W \le x \le 4W$.



Problem 2 continues on the next page

Problem 2 continued

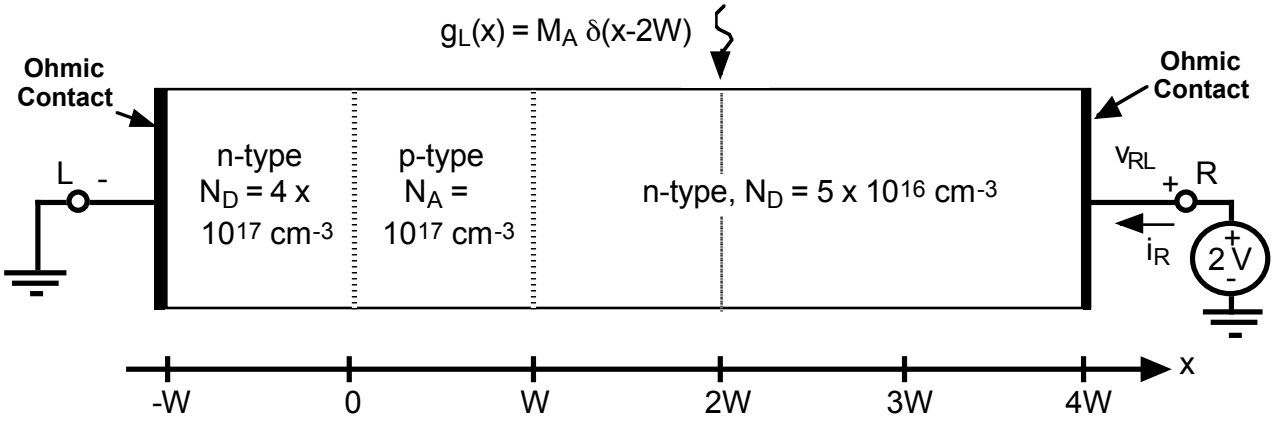
c) [5 pts] On the axes provided plot $J_e(x)$ and $J_h(x)$ for **all** x.



d) [4 pts] What is the current in at Terminal R, i_R? The cross section area is A cm^2.

i_R = _____ Amps

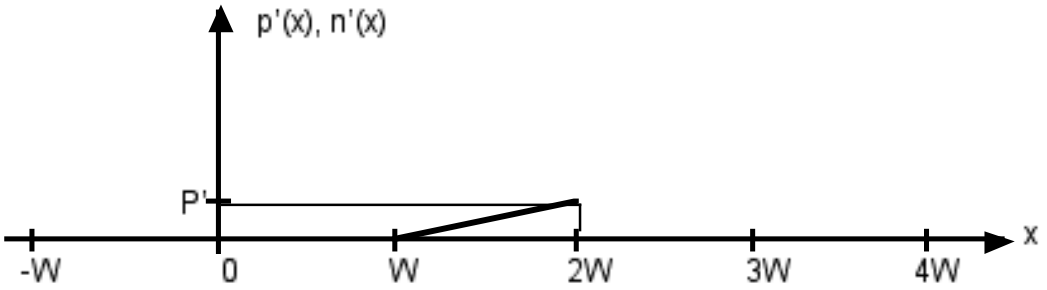
Next consider the illuminated BJT structure illustrated below. It is identical to our original diode with a second n-type region added to the left end. A voltage, V_{RL}, is applied to the structure as indicated; V_{RL} = 2 Volts.

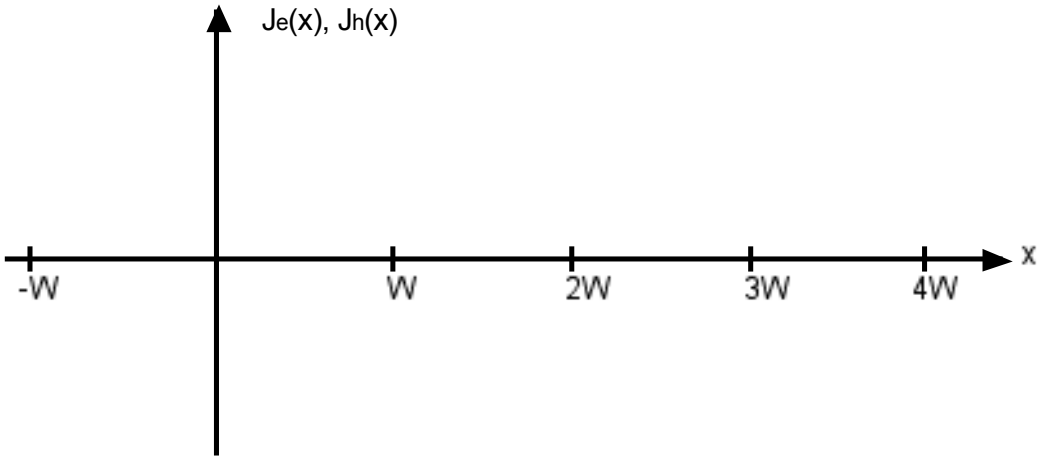


Problem 2 continues on the next page

Problem 2 continued

e) [8 pts] On the axes provided, sketch the excess minority carrier populations, and the total hole and electron currents in the illuminated device with the bias v_{RL} applied. Also, find an expression for the current through the device, i_R. The cross section area is A cm^2. Note the useful observations below.





i_R = _____ Amps

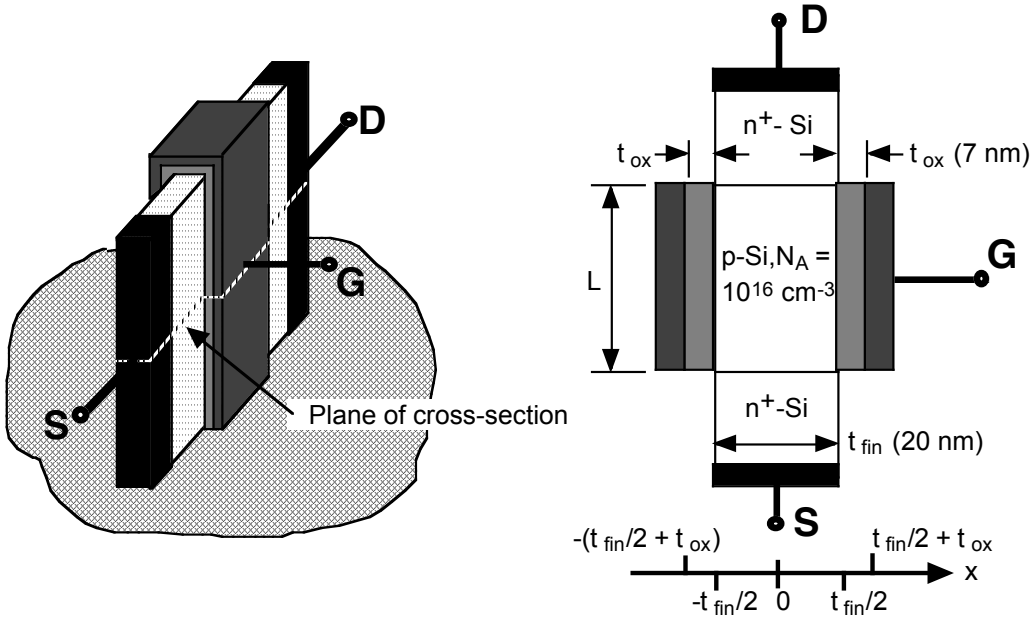
Useful observations:

1. With no base contact and infinite minority carrier lifetime, what flows into the base from the emitter must flow out through the collector; similarly what flows into the base from the collector must flow out through the emitter.
2. A portion of the 2 V bias will reverse bias the base-collector junction and a portion will forward biases the base-emitter junction. The size of the latter portion depends on the size of the emitter currents needed to yield a self-consistent situation.

End of Problem 2

Problem 3 - (25 points)

The finFET is a MOSFET structure that is receiving a large amount of research and development attention because it offers promise for solving the challenge of making Si MOSFETs even smaller (i.e., channel lengths under 20 nm). It is basically a vertical rectangular bar (fin) of silicon sitting on an insulating surface with source and drain regions on either end and with a gate dielectric and metal draped over its middle, as illustrated in the cartoon below left. The cross-section of a finFET you can use for a 6.012-type one-dimensional electrostatic analysis is shown on the right.



Looking at the cross-sectional figure, note several features: there is no body contact, B; the structure is symmetrical left to right; and the channel inversion layer forms along the upper, left-hand, and right-hand oxide-semiconductor interfaces.

a) [2 pts] Is the finFET illustrated above NMOS or PMOS?

_____ NMOS _____ PMOS because

b) [4 pts] Consider first a conventional planar MOS capacitor fabricated on a thick p-type silicon wafer with $N_A = 10^{16}$ cm^{-3}.

i) In this structure, how wide would the depletion region be at the threshold of strong inversion, $v_{GS} = V_T$?

x_D @ $v_{GS} = V_T$: _____ nm

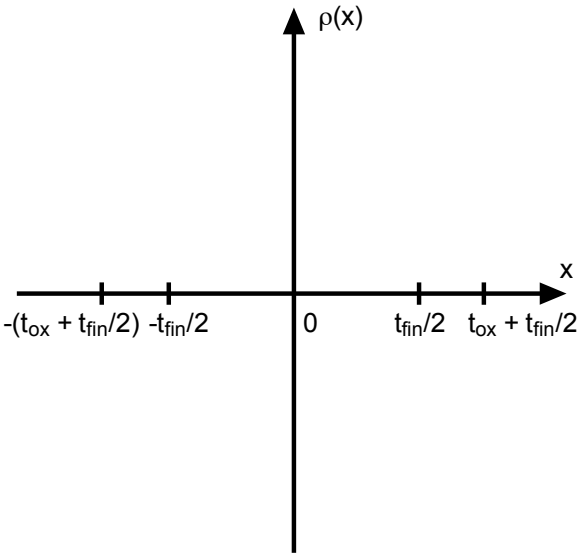
ii) The width of the fin in a typical finFET, t_{FIN}, is 20nm, or less. How does this compare with your answer in part i), and what does it indicate about the finFET (in which N_A also is 10^{16} cm^{-3}) at threshold?

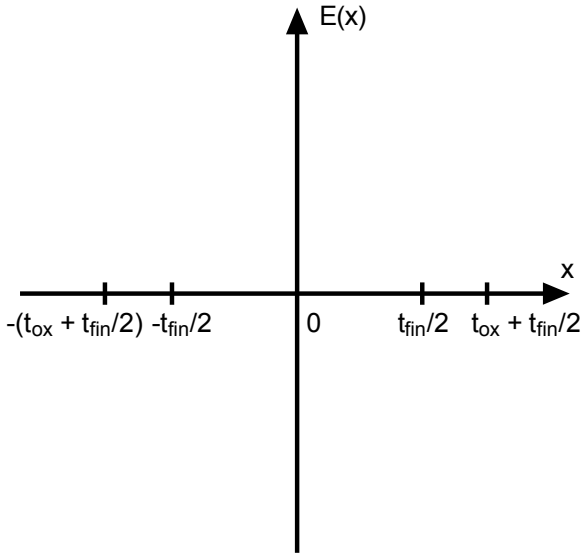
Problem 3 continues on the next page

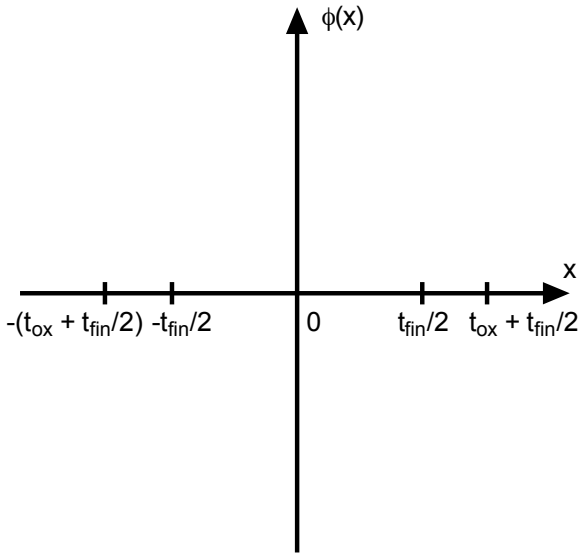
Problem 3 continued

c) [10 pts] On the axes provided below plot the net charge density, $\rho(x)$, electric field, $E(x)$, and electrostatic potential, $\phi(x)$, in this finFET from within the gate metal on the left into the gate metal on the right, when it is biased at threshold, $v_{GS} = V_T$, i.e., just at the onset of strong inversion.

Assume that the oxide thickness, t_{ox}, is 7 nm, the fin thickness, t_{fin}, is 20 nm, the silicon doping level, N_A, is 10^{16} cm^{-3}, and the electrostatic potential of the metal, ϕ_m,is -0.3 V. Use symmetry where possible to make your work easier.







Problem 3 continues on the next page

Problem 3 continued

d) [3 pts] What is the flatband voltage, V_{FB}, of this finFET?

V_{FB} = _____ V

e) [3 pts] What is the threshold voltage, V_T, of this finFET?

V_T = _____ V

f) [3 pts] The fact that the depletion region under the gate of a finFET can only be so large has important consequences for several MOSFET properties. In 25 words or less, explain what the consequence is for the following parameters:

i) The voltage-dependent current source $g_{mb}v_{bs}$ in the MOSFET linear equivalent circuit.

ii) The factor "α" in the drain current expression for a MOSFET operating in the strong inversion region.

iii) The factor "n" in the drain current expression for a MOSFET operating in the sub-threshold region.

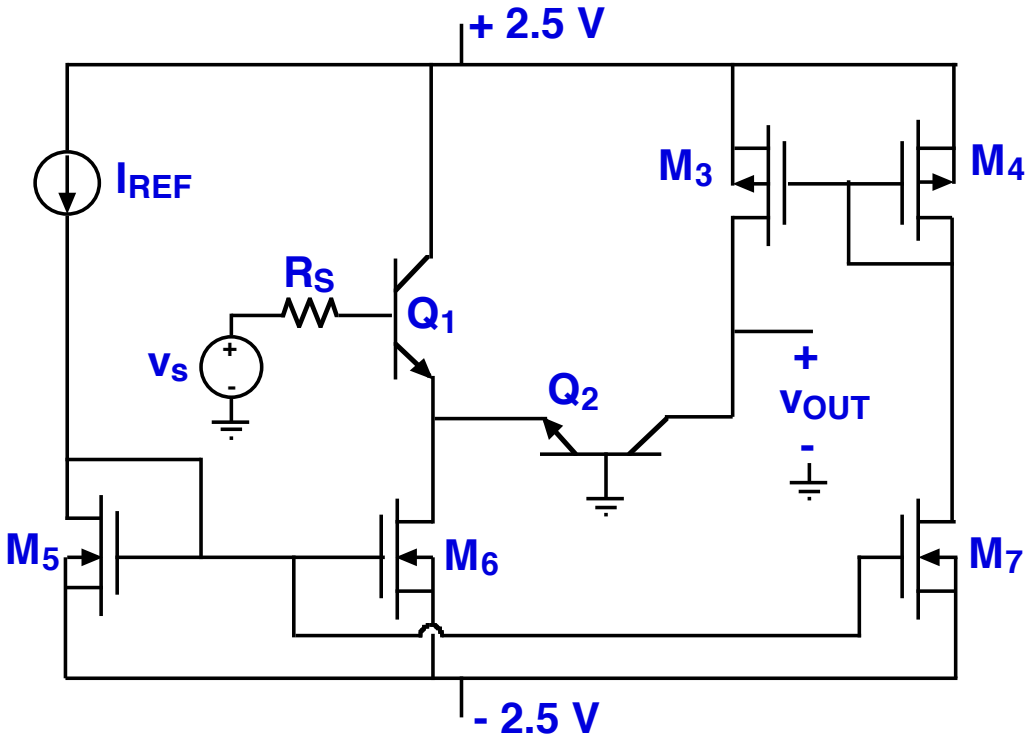
End of Problem 3

Problem 4 - (25 points)

This problem will study the amplifier shown below with two npn BJTs (Q1 and Q2), two p-MOSFETs (M3 and M4), and three n-MOSFETs (M5, M6, and M7). In this amplifier the device dimensions are as follow: $(W/L)_3 = (W/L)_4 = (W/L)_5 = (W/L)_6 = 50\mu m/4\mu m$, and $I_{REF} = 100\ \mu A$. In addition, we know the following device parameters:

MOSFETs:
- $\mu_e C_{ox} = 50\ \mu A/V^2$
- $\mu_h C_{ox} = 25\ \mu A/V^2$
- $V_{Tn} = -V_{Tp} = 1\ V$
- $C_{ox} = 2.3\ fF/\mu m^2$
- $C_{ov} = 0.5\ fF/\mu m$
- $V_{An} = -V_{Ap} = 20\ V\ @\ L = 2\ \mu m$

npn BJTs:
- $I_{BS} = 10^{-17}\ A$
- $\beta_F = 100$
- $C_\pi \approx 15\ fF$
- $C_\mu \approx 10\ fF$
- $V_{CE,sat} = 0.3\ V$
- $V_A = 25\ V$



a) [3 pts] Determine the width to length ratio of n-channel MOSFET M7, $(W/L)_7$, so that the amplifier is biased with all the devices operating in the saturation region and $I_{C1} = I_{C2} = 50\ \mu A$.

$(W/L)_7$: _____

Problem 4 continues on the next page

Problem 4 continued

b) [4 pts] What are the largest possible positive and negative output voltage swings, $v_{OUT(max)}$ and $v_{OUT(min)}$?

$V_{OUT(max)}$ = _____ V

$V_{OUT(min)}$ = _____ V

c) [6 pts] In the space below, draw the small signal linear equivalent circuit of this amplifier and identify the value of each component.

d) [3 pts] Find mid-band voltage gain, $A_v = v_{out}/v_s$ of this amplifier when the source resistance, R_S, is = 5kΩ.

A_v = _____

Problem 4 continues on the next page.

Problem 4 continued

e) [3 pts] Calculate the quiescent power dissipation, i.e. when $v_s = 0$ V in this amplifier.

Quiescent power dissipation = _____ W

f) [3 pts] Design the current source I_{REF}.

g) [3 pts] Estimate the high frequency roll-off of this amplifier, ω_{HI}, with the output capacitively connected to a load resistance of 100 Ohms. Only consider the parasitic capacitances of Q_1 and Q_2 in your estimation.

ω_{HI} = _____ radians/s

End of Problem 4; end of Final Exam. Happy Holidays.

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