MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.012 MICROELECTRONIC DEVICES AND CIRCUITS

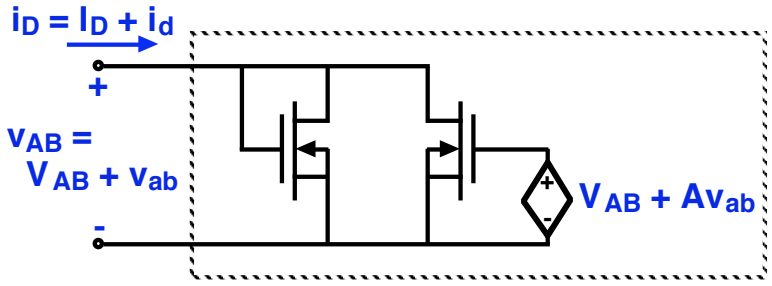
Problem Set No. 10

Issued: November 13, 2009 **Due:** November 20, 2009

Design Problem: The design problem will be distributed on Wednesday, November 18. Your solution will be due on Friday, December 4 by 5 p.m. Note that you should neglect the Early effect when doing your large signal analyses, but you must include it (g_o) in your LEC analyses.

Reading Assignments:
Lecture 19 (11/17/09) - Chap. 12 (12.1, 12.2, 12.3)
Lecture 20 (11/19/09) - Chap. 12 (12.4, 12.5), Chap. 13
Lecture 21 (11/24/09) - Chap. 13, Notes

Problem 1 – The Lee Load, which will be used in the first stage of the design problem, can be modeled by the two terminal circuit shown below containing a voltage dependent voltage source whose value is different for difference- or common-mode inputs to the associated differential stage. Consequently the LEC for the load is different for difference- and common-mode analysis.



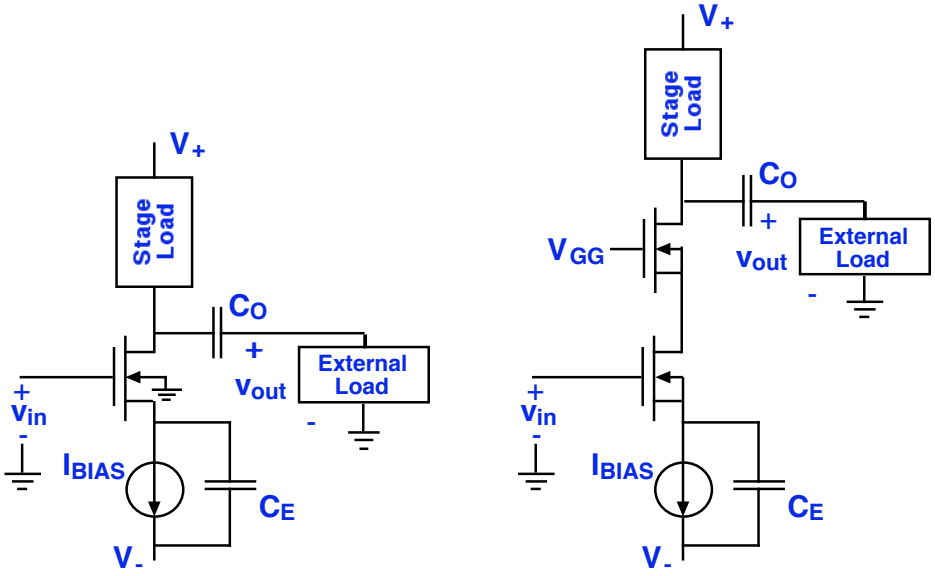
The two n-MOS transistors in this circuit are identical with the same dimensions and values of K, V_T, and λ. Assume that $V_{AB} > V_T$ so both transistors are active (and operating in saturation).

a) Find the linear equivalent conductance of this circuit when A = -1. This is $g_{oLL,dm}$, the equivalent conductance of the Lee Load in a difference mode half circuit (i.e., $1/r_{oLL,dm}$ in the upper half circuit on Slide 23 of Lecture 20).

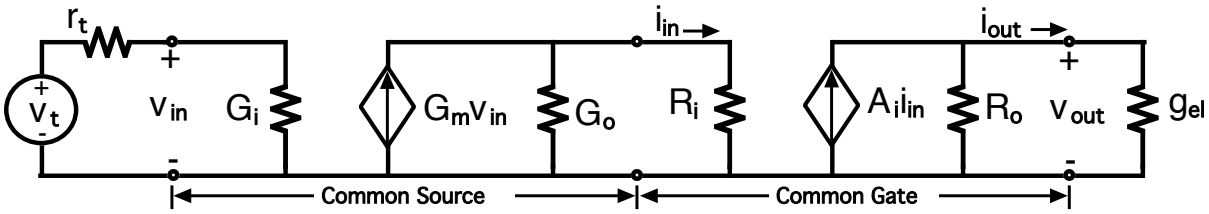
b) Find the linear equivalent conductance of this circuit when A = +1. This is $g_{oLL,cm}$, the equivalent conductance of the Lee Load in a common mode half circuit (i.e., $1/r_{oLL,cm}$ in the lower half circuit on Slide 23 of Lecture 20).

Use your results in Parts a and b to find expressions for A_{vd} and A_{vc} of the first stage of the design problem circuit in terms of g_{m4}, g_{m8}, g_{o4}, g_{o8}, and g_{o10}. Then write your expressions in terms of the K's, V_A's, I_D's, and V_{GS}'s. Eliminate I_D from your expressions and then calculate the maximum possible value of $|A_{vd}|$ and of $|A_{vd}|/|A_{vc}|$.

Problem 2 - Consider the two-stage amplifier with a common-source first stage and a common-gate second stage shown on the right below.



Use the two-port models for the common-source and common-gate stages (shown below) to compare the voltage gain and output resistance of this two-stage amplifier to the single common-source amplifier shown above on the left.



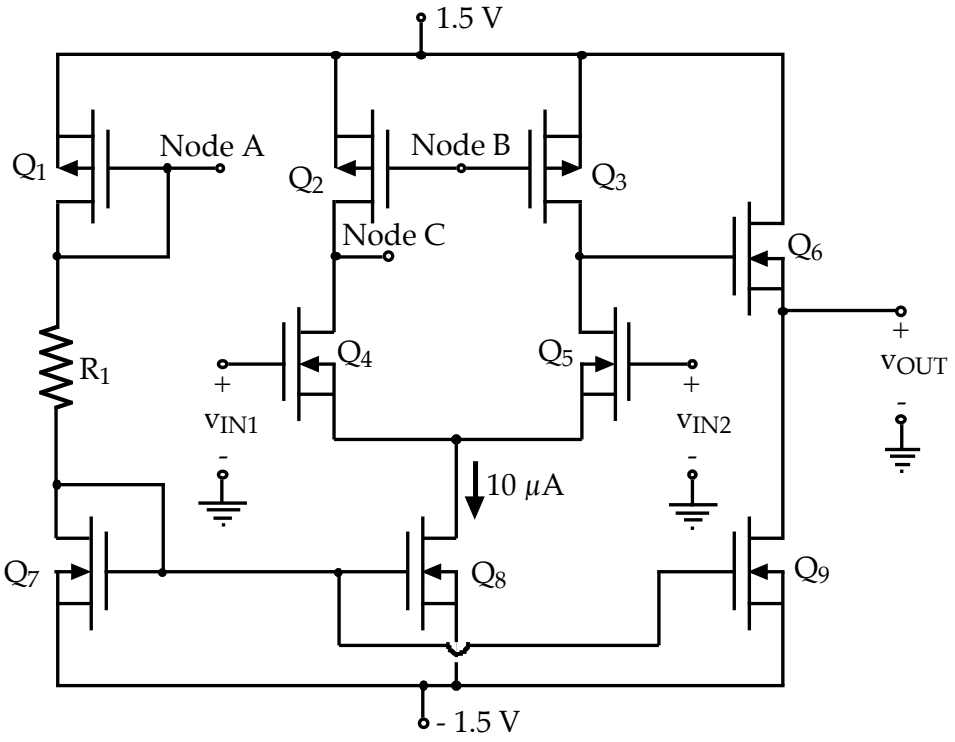
You can find expressions for the elements in each of these two-port models on the foils for Lecture 18. Note that the substrate of the transistor in the common gate stage has been connected to the source so the g_{mb} factor should be deleted from the expressions also assume that the stage load conductance, g_{sl}, is negligibly small so you can say it is zero (so, for example, R_{in} is simply $1/g_m$, and the current gain is identically one).

a) Calculate the voltage gain, v_{out}/v_{in}, of the two-stage amplifier and compare it to that of the single common-source stage.

b) Calculate the output resistance, R_o, of the two-stage amplifier and compare it to that of the single common-source stage.

Problem 3 - The circuit shown at the top of the next page contains n-channel and p-channel MOSFETs all of which have the same gate length, $L = L_{min}$; all the gate widths, however, are not equal, but they are all integer multiples of W_{min}. All have an Early voltage, V_A, of 10 V; the magnitude of all of their threshold voltages, V_T, is 0.5 V; and all must be biased with $|V_{GS} - V_T| \geq 0.1$ V.

The K-factor of an n-channel MOSFET with $L = L_{min}$ and $W = W_{min}$ is 250 $\mu A/V^2$, and the K-factor of a p-channel MOSFET with $L = L_{min}$ and $W = W_{min}$ is 125 $\mu A/V^2$.



The drain current of Q_8 is known to be 10 μA, and W_7, the width of Q_7, is known to be W_{min}. The resistor R_1 has been selected so that Q_1 and Q_7 are biased with $|V_{GS} - V_T| = 0.1$ V. The widths of Q_2, Q_3, Q_4, and Q_5 have been chosen so that for each of them $|V_{GS} - V_T| = 0.1$ V when $v_{IN1} = v_{IN2} = 0$.

For Parts a), b), c) and d) connect Node B to Node A.

a) This part concerns the bias chain Q_1, R_1, and Q_7.
   i) What is I_{D7}, the drain current of Q_7, and that is W_1, the width of Q_1?
   ii) What is the value of the resistor R_1?

b) What is the most negative common mode voltage, v_{IC}, that can be applied to the input terminals before one or more transistors in the amplifier are forced out of saturation? Remember that Node B is connected to Node A

c) What is the small signal output, v_{out}, with the following difference-mode inputs: $v_{in1} = v_a$ and $v_{in2} = -v_a$? Give your answer in three forms: (i) an expression in terms of the g_m's and g_o's of the relevant transistors, (ii) an expression in terms of the bias points of the relevant transistors, and (iii) a numerical value. Assume the voltage gain of the source-follower output stage (Q_6) is 1. Remember: Node B is connected to Node A.

d) Draw the linear equivalent half-circuits for this amplifier for the following common-mode inputs: $v_{in1} = v_{in2} = v_{ic}$. Label your drawings in terms of the g_m's and g_o's of the relevant transistors. You do not need to find numerical values for the elements. Recall that Node B is connected to Node A.

e) How will your answers in Part c) change if Node B is connected to Node C, instead of to Node A? State the change and give the name of this circuit topology, i.e., of this connection.

For the rest of this problem leave Node B connected to Node C.

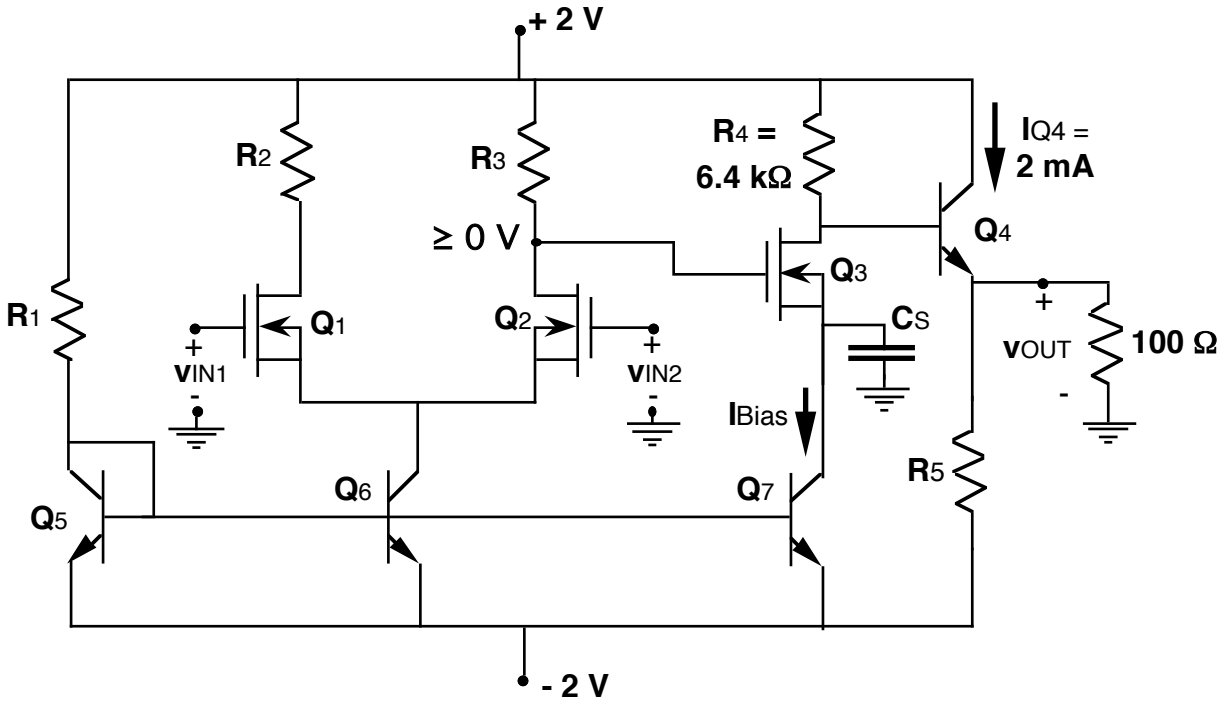
f) Size Q_6 and Q_9 so that the output resistance of this amplifier is 1000 Ohms AND so that the quiescent output voltage (v_{OUT} with $v_{IN1} = v_{IN2} = 0$) is 0. The widths should be integer multiples of W_{min}.

g) For your design in Part f, what is the most negative value v_{OUT} can have if the output is attached to a 1 kOhm load resistor? Hint: This occurs when v_{GS6} gets so small that Q_6 cuts off and all of the drain current of Q_9 (the current sink) is drawn from ground through the 1 kOhm load resistor.

h) For your design in Part f, what is the most positive value v_{OUT} can have if the output is attached to a 1 kOhm load resistor? This occurs when the voltage on the gate of Q_6 is so high that Q_3 is pushed out of saturation because v_{SD3} becomes too small. What is v_{GS3} at this maximum value of v_{OUT}?

Note: Parts g and h should show you why a push-pull output stage is used in the design problem circuit.

Problem 4 - Consider the differential amplifier circuit illustrated below. In this circuit the three n-channel MOSFETs are identical; they have a threshold voltage, V_T, of 1 V, a drain current in saturation of $2.5(v_{GS} - V_T)^2$ mA, and an Early voltage of 10 V. The MOSFETS should be operated with $(v_{GS} - V_T) \geq 0.2$ V. The npn bipolar junction transistors (BJTs) all have forward betas, β_F, of 100 and an Early voltage of 50 V. The BJT sizes have been adjusted to that to a good approximation you may use $V_{BE,ON} = 0.6$ V; $V_{CE,SAT} = 0.2$ V. Assume C_S is a short at mid-band frequencies, and R_2 and R_3 are identical.



Note that value of the resistor R_4, the quiescent collector current on Q_4, and minimum quiescent voltage on the gate of Q_3 are indicated on the schematic, as are the supply voltages.

a) What must the bias level (I_{Bias}) on Q_3 be to have a quiescent output voltage of approximately 0 V? (Assume that the quiescent collector current of Q_4 is 2 mA, as indicated, and do not forget its base current.)

b) Select R_5 be to be consistent with a quiescent collector current in Q_4 of 2 mA, and a quiescent output voltage of approximately 0 V.

c) Select R_1 to give a bias current through Q_5 of 1 mA. You may ignor the base currents of Q_5, Q_6, and Q_7.

d) i) Draw a small signal linear equivalent <u>half</u> circuit one could use to calculate the signal voltage on the gate of Q_3 due to the difference-mode input signal, $v_{in1} - v_{in2}$. Find an expression for this voltage in terms of incremental linear equivalent circuit model parameters.

ii) Write an expression for the differential-mode voltage gain of the differential stage (Q_1, Q_2) in terms of the resistors, the MOSFET K-factors, and the quiescent bias levels of Q_1 and Q_2. Select R_2 (= R_3) and the drain current of Q_1 and Q_2 to maximize this voltage gain (magnitude).

e) Suppose you can replace R_2 and R_3 with a current mirror made with p-channel MOSFETs with $|V_T| = 1$ V and $|V_A| = 20$ V. Draw the schematic of such a current mirror, and calculate what impact this would have on the voltage gain.

f) Looking at the output stage, what are the most positive and negative values of v_{out} possible? Explain your answers.

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