Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Circuits & Electronics
Spring 2004

Quiz #2

1 April 2004

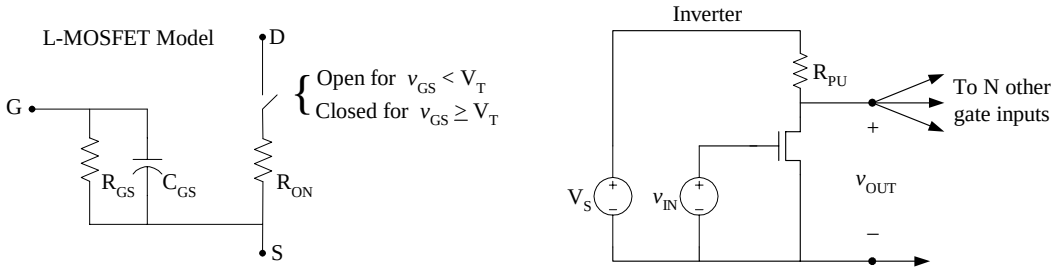
Name: _____

- Please put your name in the space provided above, and circle the name of your recitation instructor together with the time of your recitation.
- Do your work for each question within the boundaries of the question. When finished, write your answer to each question in the corresponding answer box that follows the question.
- This is a closed-book quiz, but calculators are allowed.
- Graded quizzes will be returned in recitation on Wednesday April 7. If you do not attend recitation on that day, then it is your responsibility to get your quiz from your recitation instructor. You will have until recitation on Wednesday April 21 to request a quiz grading review, regardless of whether or not you attend recitation on Wednesday April 7 and take back your quiz. If you wish to have your quiz grade reviewed, you must return your quiz to your recitation instructor, within the two week period, together with a written explanation of why you think a grading mistake was made. This is the only way in which a quiz grade will be reviewed.
- Good luck!

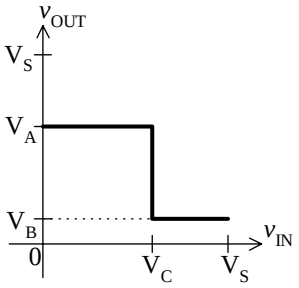
Problem 1	Problem 2	Problem 3	Total Grade

Problem 1 – 35%

A hypothetical "leaky" MOSFET (L-MOSFET) is modeled with the additional gate-to-source resistance R_{GS} as shown below. Also shown below is an inverter constructed using the L-MOSFET. *Assume that the inverter drives N identical inverters from its output, as indicated.* Given this load, the inverter is required to obey the standard static discipline defined by $0 < V_{OL} < V_{IL} < V_{IH} < V_{OH} < V_S$.



(1A) The static ($C_{GS} = 0$) input-output characteristic of the inverter is as shown below. Determine the voltages V_A, V_B and V_C that define this characteristic. Express the voltages in terms of V_S, R_{PU}, N and the L-MOSFET parameters.



V_A:

V_B:

V_C :

(1B) In terms of the static discipline parameters ($V_{\rm OL}$, $V_{\rm IL}$, $V_{\rm IH}$ and $V_{\rm OH}$), determine the voltage range within which the threshold voltage $V_{\rm T}$ must be designed for the inverter to obey the static ($C_{\rm GS} = 0$) discipline at its input.

$\leq V_{\rm T} \leq$

(1C) Determine the resistance range within which the pull-up resistance $R_{\rm PU}$ must be designed for the inverter to obey the standard static ($C_{\rm GS} = 0$) discipline at its output. Express the range in terms of $V_{\rm S}$, N, the L-MOSFET parameters and the static discipline parameters.

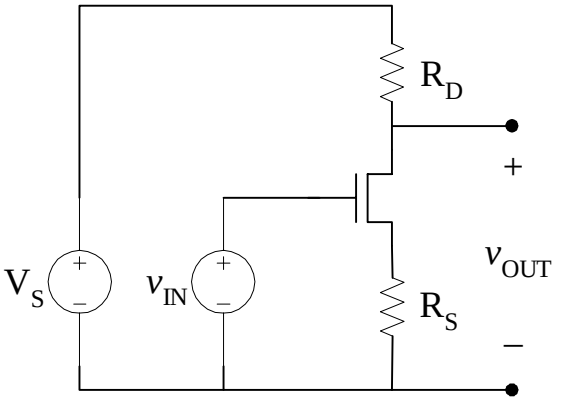
$$\leq R_{\rm PU} \leq$$

(1D) Assume that $v_{\rm IN}(t) > V_{\rm T}$ for $t < 0$ so that the L-MOSFET switch is initially closed. For $t \geq 0$, $v_{\rm IN}$ steps to $v_{\rm IN}(t) < V_{\rm T}$ so that the L-MOSFET switch opens. For this input, determine the dynamic ($C_{\rm GS} > 0$) response of the inverter. That is, determine $v_{\rm OUT}(t)$ for $t \geq 0$. Express $v_{\rm OUT}$ in terms of $V_{\rm S}$, $R_{\rm PU}$, N, the L-MOSFET parameters. You may also use $V_{\rm A}$, $V_{\rm B}$ and $V_{\rm C}$ from Part 1A in your answer.

$v_{\rm OUT}(t \geq 0)$:

Problem 2 – 30%

This problem concerns the analysis of the MOSFET amplifier shown below. For the purposes of this analysis, assume that the MOSFET operates in its saturation region. The corresponding MOSFET characteristics are also given below.



Saturation Region:

$v_{DS} \geq v_{GS} - V_T \geq 0$

$i_D = 0.5K\,(v_{GS} - V_T)^2$

(2A) Determine v_{OUT} as a function of v_{IN}. Express v_{OUT} in terms of the circuit parameters and the MOSFET parameters.

v_{OUT}:

(2B) Let $v_{\rm IN} = V_{\rm IN} + v_{\rm in}$ where $V_{\rm IN}$ and $v_{\rm in}$ are the large-signal and small-signal components of $v_{\rm IN}$, respectively. Further, let $v_{\rm OUT} = V_{\rm OUT} + v_{\rm out}$ where $V_{\rm OUT}$ and $v_{\rm out}$ are the large-signal and small-signal components of $v_{\rm OUT}$, respectively. Assume that the amplifier is biased with a value of $V_{\rm IN}$ that results in saturated operation of the MOSFET. For this case, draw the circuit that models the small-signal behavior of the amplifier, and that can be used to determine $v_{\rm out}$ from $v_{\rm in}$. Clearly label the components in the model.

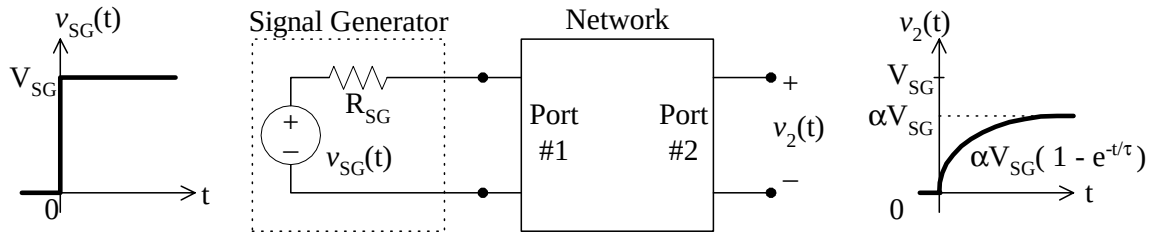
Model:

(2C) Determine the small-signal gain $v_{\text{out}}/v_{\text{in}}$ of the amplifier. Express the gain in terms of the amplifier parameters, the MOSFET parameters and the bias voltage V_{IN}.

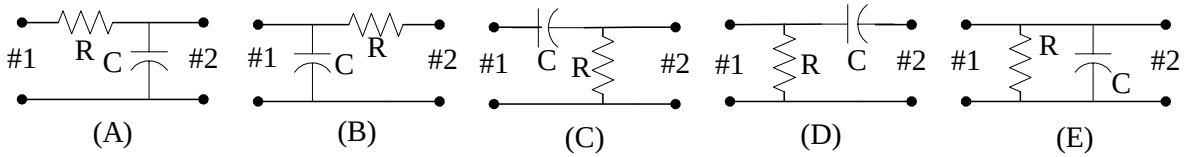
$v_{\text{out}}/v_{\text{in}}$:

Problem 3 – 35%

A signal generator having Thevenin resistance $R_{\rm SG}$ is connected to Port #1 of a two-port network as shown below. At $t = 0$, the Thevenin voltage $v_{\rm SG}(t)$ of the signal generator takes a step from zero to $V_{\rm SG}$, and the voltage $v_2(t)$ is measured at Port #2 as shown below with the port open-circuited. Note that α is a unitless constant satisfying $0 < \alpha < 1$, and τ is a time constant. Assume that the Thevenin voltage of the signal generator is zero for a very long time prior to the step.

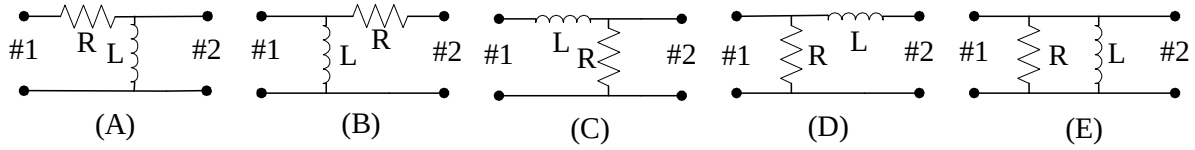


(3A) Which of the following could be the two-port network?



Network (Circle One):	A	B	C	D	E

(3B) Which of the following could be the two-port network?

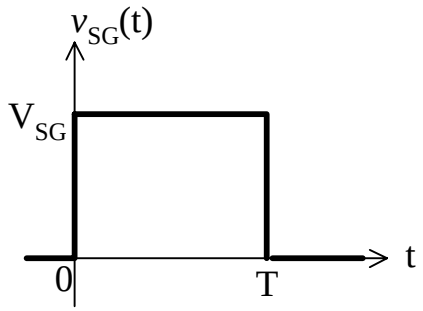


Network (Circle One):	A	B	C	D	E

(3C) Determine the values of R and L in the network you chose in Part 3B. Express the values in terms of V_{SG}, R_{SG}, α and τ.

R:	L:

(3D) The Thevenin voltage $v_{SG}(t)$ of the signal generator now produces the pulse having amplitude V_{SG} and duration T shown below. Determine the voltage $v_2(t)$ measured at Port #2 for $t \geq 0$ with the port open-circuited. Express $v_2(t)$ in terms of V_{SG}, R_{SG}, T, τ and α. Assume that the Thevenin voltage of the signal generator is zero for a very long time prior to the pulse.



$v_2(t \geq 0)$: